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November 2016

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VIAS

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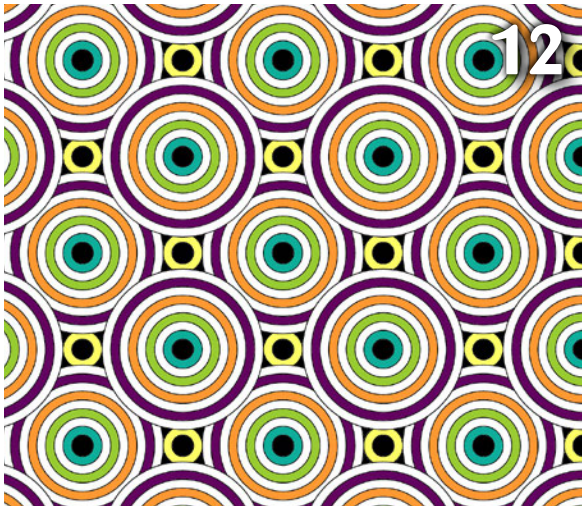

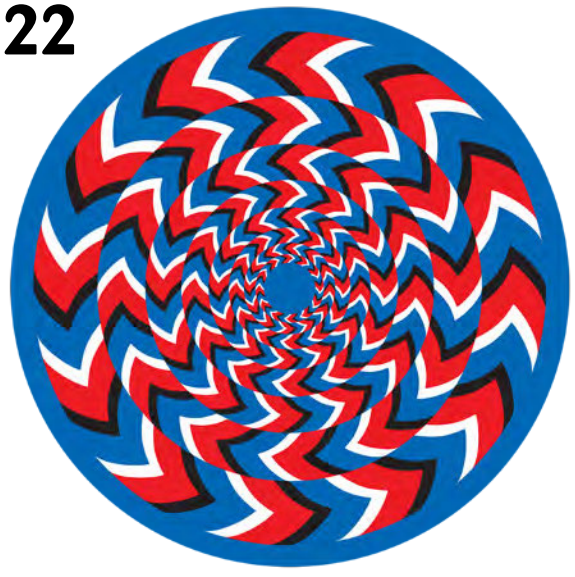

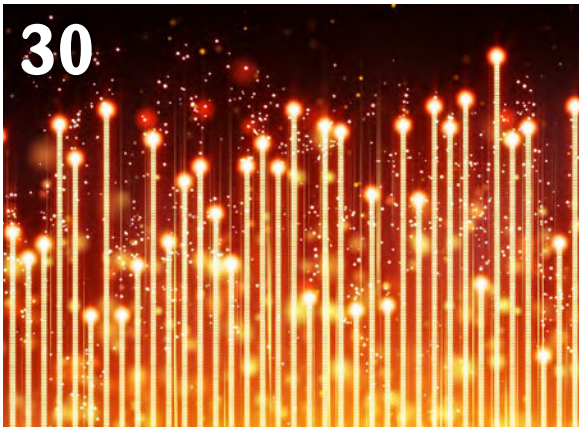

Vias

Time after time, we've heard about issues that continue to challenge readers like you, and some of the most often cited problem areas are related to vias. Whether blind, buried, microvias, thermal vias, landless or backdrilled, vias are a big problem. In this issue, David Wolf of Conductor Analysis Technologies takes us through the company's analysis program and highlights some of the trends and problems areas he sees in via structures. Mark Thompson of Prototron Circuits focuses on some typical via missteps and miscues he sees in the CAM department. Martyn Gaudion of Polar Instruments discusses vias, modelling and signal integrity. And David Warren of Sunstone Circuits takes us through the company's move into the RF and microwave space.

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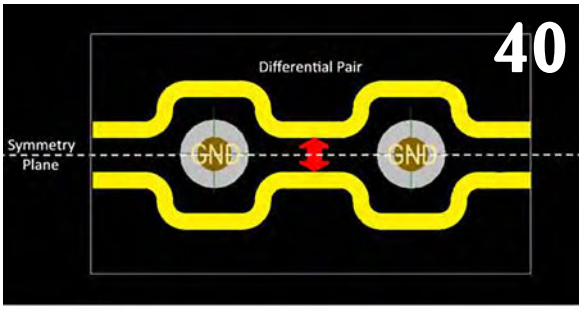

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The Hole Truth

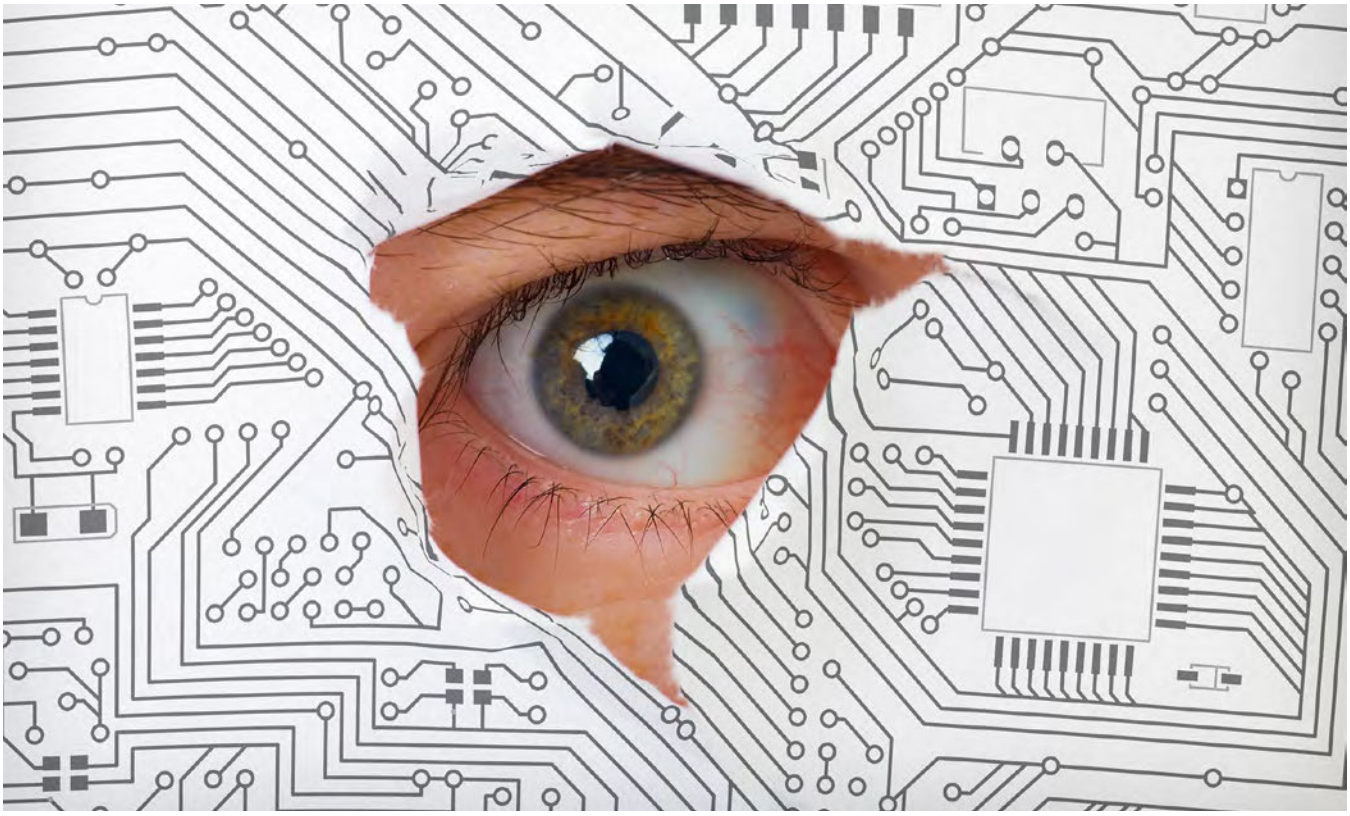
by Andy Shaughnessy
I-CONNECT007

For such a simple structure, the PCB via certainly stirs up more than its share of intrigue.

The via is another one of those topics that pop up in our reader surveys when we ask about your ongoing challenges. And it's not just the blind and buried vias that draw readers' attention. Something as basic as a hole drilled through a circuit board can generate a whole lot of controversy.

To get a handle on this issue, we sent readers a survey dedicated solely to vias. We asked readers to describe their greatest via challenges, and the comments told the tale. Here is a small sample of the replies:

- Understanding the PCB manufacturing process
- Impedance matching
- Routing high I/O .65 mm pitch vias
- Tolerances or limitations of the PCB house
- The cost of blind and buried
- Via-in-pad
- Finding the smallest via that can be created with a high yield
- The correct size for HDI and IPC Class 3
- The cost of filling and plating over them
- Not enough pad for annular ring in the design
- Designers do not understand aspect ratio.
- Blind via plating technology
- Vias under components
- Tenting vias
- In-house politics: cost, fear of the unfamiliar
- Reliability concerns due to thermal cycling
- Vias with large board thicknesses
- Strength when temperature cycled
- Cost of standard vias vs. state of the art



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Other bits of interesting info from our via survey:

- About 85% of respondents said they use blind and/or buried vias
- 83% use thermal vias
- Only one respondent uses landless vias; many said their fabricator couldn't manufacture them if they asked
- Dog bone and via-in-pad were the most popular methods to breakout vias for BGAs
- Many readers have never used or even heard of landless vias or back-drilling vias

We asked what you wanted to know, and as usual, you were not shy. In a typical cry for help, one respondent asked for an "inexpensive method to increase packing density before resorting to microvias and/or blind and buried vias." Another asked, "What is the difference between tented and capped vias?" Still another wondered, "How do we form vias that are conducive to plating?"

As you can see, vias are subject to all sorts of challenges—electrical, chemical, and mechanical—all of which can lead to increased cost and lower manufacturing yields. Much of this confusion seems to be caused by a lack of information about fabricators' via capabilities. To paraphrase an answer given by several respondents, "What is the smallest via that can be reliably manufactured in North America, and elsewhere?"

All of which brings us to our November issue on vias. This month, we have a cover story by David Wolf, vice president of technical marketing for Conductor Analysis Technologies. Wolf takes us through the company's analysis program and highlights some of the trends and problems areas he sees in via structures. He also details his work with IPC on the Process Capability and Relative Reliability (PCQR^2) assessment.

Mark Thompson of Prototron Circuits explains some of the typical via missteps and miscues that he sees in from his viewpoint in the CAM department, including when to use methods such as via stitching, via-in-pad, epoxy fill. He also provides a primer on calling out tolerances for vias.

Martyn Gaudion of Polar Instruments discusses the link between vias, modelling and signal integrity, with a look at what a transmission line signal "sees" as it enters a badly designed single-ended via.

We also have an interview with Sunstone Circuits' David Warren, who discusses the company's shift into the RF and microwave market, and how Sunstone plans to gain market share in this competitive arena. It's hard to believe that it's November, partly because it's still 75° every day here in Atlanta. But DesignCon and IPC APEX EXPO are just around the corner. I'll see you next month. **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 17 years. He can be reached by clicking here.

Salty Batteries

Researchers report in the journal Angewandte Chemie that a highly concentrated electrolyte solution may make the sodium–oxygen battery more stable, and therefore more practicable.

Sodium–oxygen cells surprisingly do not produce sodium peroxide, instead making mainly sodium superoxide (NaO2), which can be almost reversibly converted back to the elements during charging.

By using Raman spectroscopy of NaTFSI/DMSO electrolyte solutions in conjunction with computational simulations, the scientists were able to explain why this is so.

The researchers built a small battery with this system. It demonstrated good electrochemical properties and underwent 150 charge/discharge cycles without any notable loss of efficiency. In contrast, cells with a dilute electrolyte solution could only last for 6 cycles.

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CAT's David Wolf on Via Reliability Analysis

by Andy Shaughnessy

Conductor Analysis Technologies (CAT) has been analyzing test panels and coupon designs for over 20 years. CAT's analysis provides valuable, quantitative data on PCB quality and reliability, which can help designers and manufacturers trace the source of defects and non-uniformities. In this e-mail interview, Vice President of Technical Marketing David Wolf discusses some of the trends he's seeing in via structures, and the common reliability and quality issues related to vias.

***Andy Shaughnessy:** David, tell us a little about Conductor Analysis Technologies and your work with the IPC PCQR² Database.*

David Wolf: Conductor Analysis Technologies Inc. is a privately held company founded in May 1994. The company is an offshoot of a National Center for Manufacturing Sciences (NCMS) program called the Imaging Team. The first test coupon design was used for evaluating conductor and space formation process capability, hence the naming of the company.

CAT is a provider of market-critical data utilized by designers, purchasers, assemblers, and manufacturers of printed circuit boards, and by material and equipment suppliers to the printed circuit industry. Our products and services provide quantitative data on printed circuit manufacturing capability, quality, and reliability.

Results from the analysis of CAT test panel and coupon designs provide quantitative yield,

Figure 1: CAT's OM testing system.

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uniformity and reliability data that are used to measure, track, and improve processes. Our data illustrate strengths and weaknesses of processes, and points to areas requiring improvement or development. Furthermore, the data offers insight into the sources of defects and process non-uniformities, allowing for their reduction or elimination.

CAT's services include test panel and coupon design, precision electrical testing, reliability testing, and comprehensive data analysis. Whether measuring, comparing, or developing processes, we provide a standardized, independent, and documented evaluation of printed circuit board process capability, quality, and reliability.

The IPC PCQR² (Process Capability, Quality and Relative Reliability) Database, an extensive supply chain management resource, was developed by IPC and CAT in the fall of 2000 for designers, purchasers, assemblers and manufacturers of printed boards. It is based on statistical data collected from industry-developed test patterns that quantifies the capability, quality and reliability of printed board manufacturers.

PCB supplier facility benchmark data was first posted in the PCQR² Database in November 2001. Since then, 220 printed board supplier facilities have submitted one or more sets of test panels for evaluation yielding a total of more than 750 sets of test panels evaluated. Within the last 36 months, 78 different printed board supplier facilities have submitted one or more test panel designs for testing. There has been an average of 120 submissions recorded in the database over the rolling 36-month comparison period. By geographic region, the submissions over the last 36 months break down as follows: 70% from Greater China; 24% from North America; 6% from Asia/Pacific; and, 0% from Europe, Middle East & Africa.

OEMs and EMS providers can subscribe to the IPC PCQR² Database by paying an annual subscription fee. As part of that annual subscription, database subscribers have full access to all analysis reports generated from testing of each 15-panel submission from participating global PCB supplier facilities. The number of active database subscribers currently stands at 14. A total 32 different companies have subscribed to the database since its beginning.

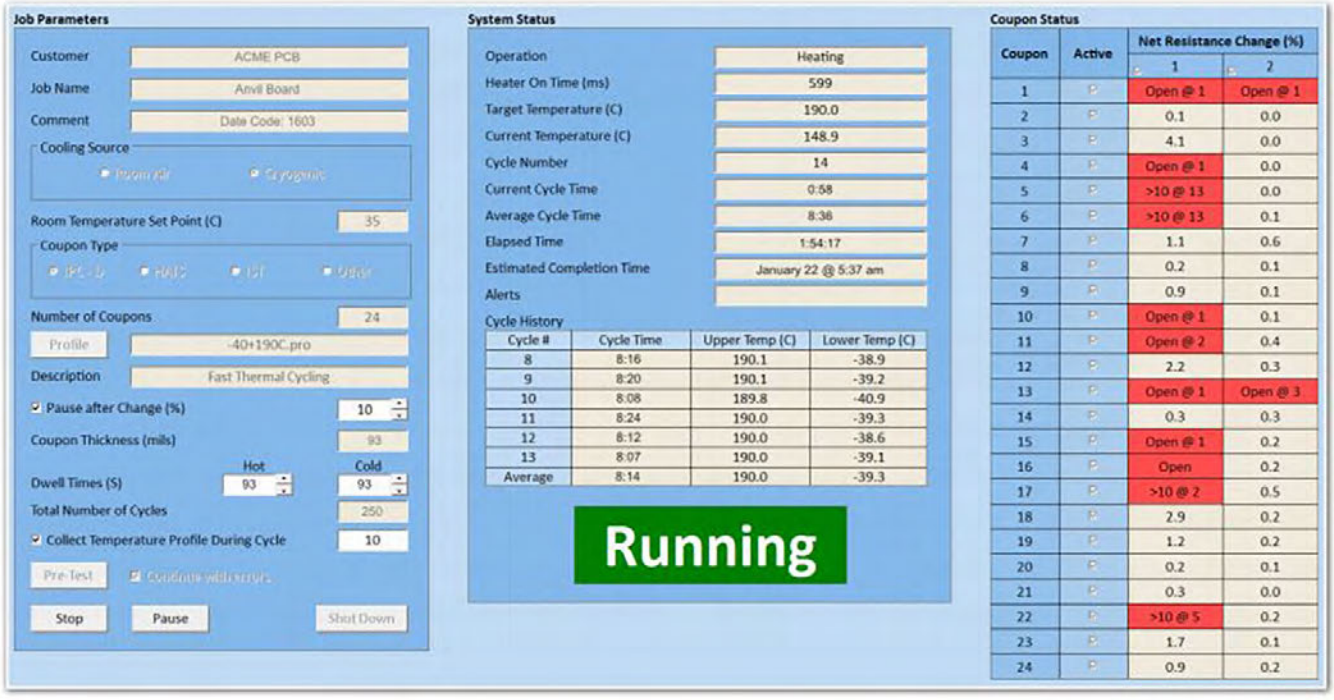

Figure 2: CAT analyzes all areas of the PCB for reliability.

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As part of the annual subscription fee, database subscribers can also sponsor up to 20 PCB supplier facility submissions during their 12-month subscription period at no additional cost.

***Shaughnessy:** Can you explain how you conduct a typical analysis of test panels and coupon designs?*

Wolf: First, let me tell you about the PCQR² test panel designs. There are eight standardized test panel designs covering three levels of technology:

- Four single lamination designs with layer counts of 6, 10,14 or 18 layers
- Two sequential lamination designs, either 14 or 24 layers, each with six different via structures
- Two HDI designs, both at 10 layers with either a 2+6+2 build-up construction or an any layer 4+2+4 stacked via construction

These process capability panel designs were developed by the IPC D-36 Subcommittee that oversees the IPC PCQR2 Database and are provided under license to IPC for use by its members and the printed circuit board community. The designs are to be used exclusively for the support of the IPC PCQR² Database. [Ed. Note: The design files for these test panel designs can be downloaded from this link.]

The designs incorporate the following structures in order to provide relevant statistics on the capability, quality, and reliability of the processes used in their manufacture:

- Outerlayer conductor/space capability
- Innerlayer conductor/space capability
- Via registration
- Via formation capability
- Via reliability
- Soldermask registration
- Single-ended controlled impedance
- Differential controlled impedance
- Conductive anodic filament
- Cross-section

All test data except controlled impedance is collected using precision resistance measurements. For impedance measurements, we use a robotic TDR tester.

CAT uses custom designed software to efficiently and accurately analyze test data and generate analysis reports and supplier facility comparison data.

***Shaughnessy:** You come across a variety of via structures. What sorts of trends are you seeing in via construction and associated via reliability? What's the breakdown of mechanical vs. laser drilled?*

Wolf: The standardized PCQR² test panel designs contain a variety of via structures which include: through vias; blind and buried microvias; buried via cores; multilayer sub-composite vias (both blind and buried); staggered and stacked microvias; and back-drilled vias. All eight of the standardized designs contain through via and 1-deep blind microvia structures using either two or four different drill diameters. The via structures and drill diameters used in the PCQR² test panel designs are dictated by the database subscribers through IPC's D-36 Subcommittee. Thus, the database is good source for global PCB supplier via formation process capability and via reliability data.

With the increasing use of finer pitched ball grid arrays, 0.012" and 0.016" [0.3 and 0.4 mm] pitch, we are seeing an increase in the number and type of blind microvia structures with drill diameters at or below 0.004" [100 mm]. Blind microvias of this drill diameter and smaller are formed with laser drilling equipment. In the PCQR² test panel designs, multilayer through and sub-composite via structures with drill diameters of 0.006" [0.15 mm] and above are typically drilled with mechanical drills.

As an extreme example, the IPC-24VH-E sequential lamination test panel design has been built at a 0.187" [4.75 mm] thickness. With 0.010" [0.25 mm] drilled through vias, the result is an 18:1 via plating aspect ratio. There are global PCB supplier facilities who have successfully formed these high aspect ratio vias and who have also demonstrated via reliability (less than 10% change in via net resistance) after 6X convection reflow assembly simulation at

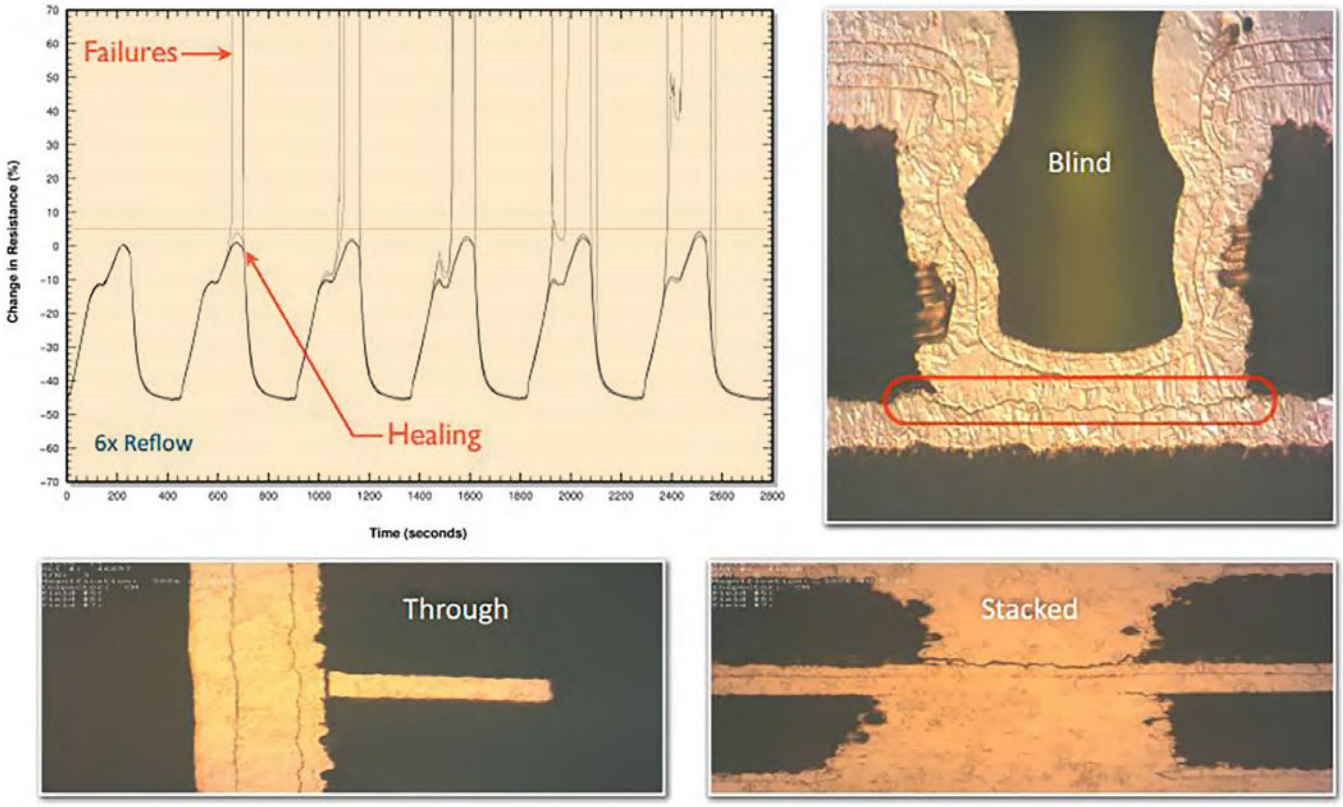

Figure 3: Through, blind and stacked vias shown after reflow simulation.

a peak temperature of 260ºC and 500 air-to-air thermal cycles from -40ºC to +145ºC.

We have collected via reliability data from many of the other standardized PCQR2 test panel designs that exhibit greater than a 5% change in via net resistance after the 6X convection reflow assembly simulation. May times those same via nets will not show failures (greater than 10% change in via net resistance) after 500 air-to-air thermal cycles; this due to the difference in z-axis expansion between +145ºC and +260ºC.

Another design trend that is becoming more common for higher layer-count boards, 14 layers and above, is the use of two-high (2+N+2) and three-high (3+N+3 or 3+N+N+3) staggered or stacked microvias on either side of multilayer sub-composite mechanically drilled vias. The unknown factor with these types of composite via structures is whether the stacked or staggered version is more reliable. The PCQR² database subscribers are requesting that these composites via structures be added to the next revision of PCQR² test panel designs so that via reliability benchmarking data can be collected. One major challenge with forming stacked via structures is registration during the sequential build-up of the via structures.

***Shaughnessy:** What are some of the more common via defects you see? How do blind/buried vias fare as far as defects?*

Wolf: For through vias and sub-composite multilayer buried or blind via structures, the defects typically seen after assembly simulation and air-to-air thermal cycling are barrel cracks, knee cracks and/or inner layer separation. In blind microvia structures, whether staggered or stacked, separation of via hole plating from the target pad is a common defect. Generally, 1-deep (layer 1-2) and 2-deep (skip layer 1-3 with no interconnect on layer 2) blind microvia structures tend to be more reliable than high aspect ratio through or sub-composite via structures. This is due to less z-axis expansion associ-

ated with the smaller depth of the drilled hole and smaller plating aspect ratios.

***Shaughnessy:** What are your thoughts on back-drilled vias?*

Wolf: Back-drilled via structures are common today in high frequency multilayer PCB applications. Back-drilling is used to remove that portion of a through via plated barrel without inner layer connections that would act as an antenna stub. Multiple depth back-drill via structures have been included in both the 14-layer and 24-layer PCQR² sequential lamination designs since January 2010. The reliability of back-drill via holes is very similar to through via holes of the same drilled diameter. The biggest challenge is drill depth control.

***Shaughnessy:** Are you seeing many landless vias, via-in-pad, or thermal vias?*

Wolf: These types of via structures have not been part of the standardized PCQR² designs. The database subscribers have not specifically requested that these types of via structures be included in the test panel designs. With landless vias and via-in-pad, the major challenge is via registration.

***Shaughnessy:** What should PCB designers know about vias and via design?*

Wolf: There are at least three areas of concern when evaluating the design of via structures:

A. Both via structure formation capability and uniformity must be controlled and repeatable before initiating via reliability studies.

For the most reliable PCB designs, use the largest via drill diameter that the PCB design will allow; this yields the lowest via hole plating aspect ratio that is easier to process. With surface mount components that have a high number of pin-outs, staggered or stacked microvia structures might be required to successfully complete circuitry routing and interconnect requirements.

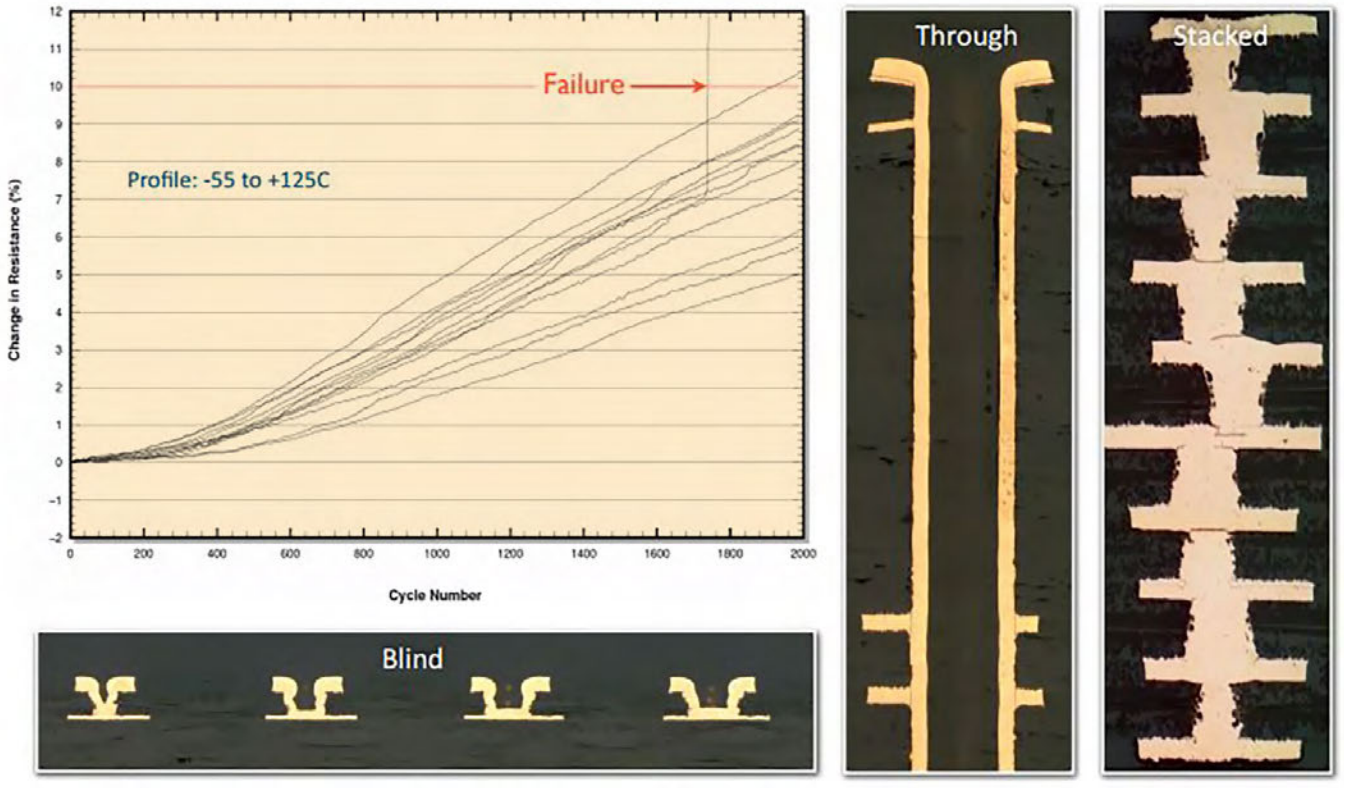

Figure 4: Blind, through and stacked vias shown after thermal cycling.

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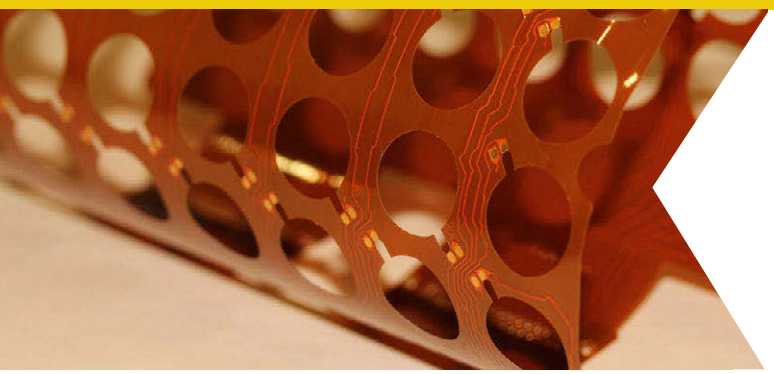

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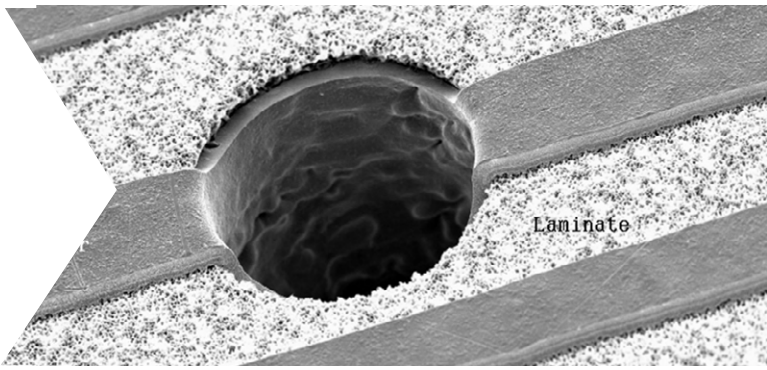

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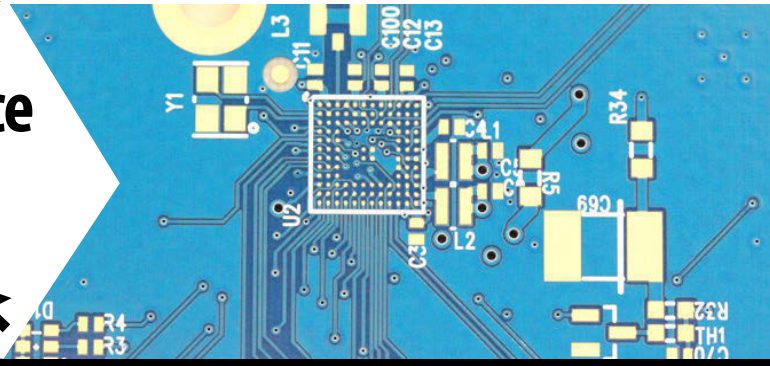

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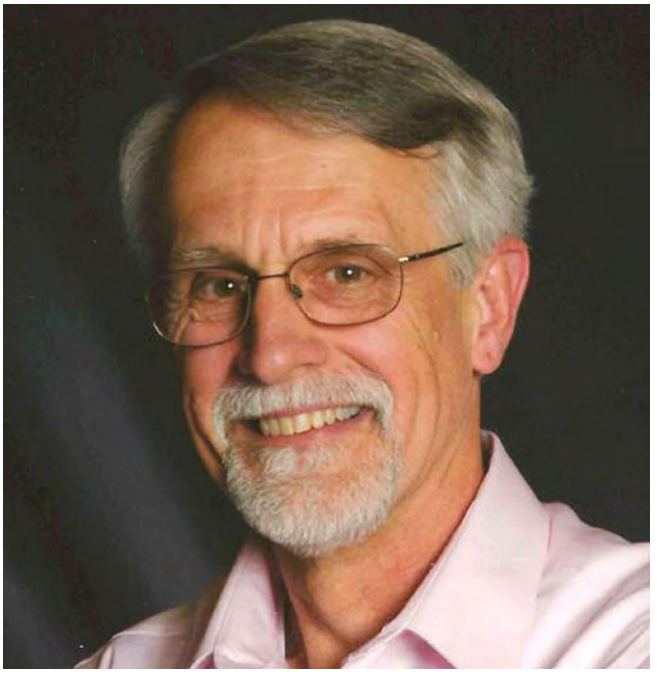

David Wolf

If a PCB supplier facility cannot consistently demonstrate excellent via formation capability (via net yields greater than 95%) and plating uniformity as measured by via net resistance (capability potential index or C_p equal to or greater than 2.0), those via structures will most likely not meet specified via reliability requirements after reflow assembly simulation and thermal cycling.

B. Not all PCB fabrication facilities can meet the same via registration requirements.

For the easiest to register via structures, design with the largest via pad annular ring that the design will allow. The industry benchmark data from PCB supplier facilities participating in the PCQR² Database shows that only a limited number of globally based PCB supplier facilities can consistently meet the following registration minimums with yields greater than 95%:

- Through and sub-composite via registration requirements of less than +/-0.005 inch [+/-125 mm]
- Blind and buried microvia registration requirements of less than +/-0.003 inch [+/-75 mm]

C. There is a direct relationship between thickness and uniformity of plated copper in via holes and the ability to consistently form associated plated layer copper features that meet target width, space, diameter and height requirements.

PCB designs that contain high aspect ratio through vias, sequential lamination, and/or copper filled microvias can require multiple panel and/or pattern plating steps. Each plating pass adds to the thickness of the resultant copper patterns. Etching of thick plated copper is more difficult than thinner copper base foil or pattern plated foil. The variability in finished conductor width and height can have a direct influence on the ability to meet controlled impedance requirements.

***Shaughnessy:** Is there anything else you'd like to add?*

Wolf: In 2013 CAT began using the OM Thermal Stress System to test both PCQR² and HATS™ via reliability coupon designs. The OM system is also capable of testing the AB/R and D coupon designs defined in IPC-2221B, Appendix A.

CAT developed the OM Thermal Stress System as a cost-effective performance based via net reliability test methodology which performs both convection reflow assembly simulation per IPC TM-650 2.6.27 and air-to-air thermal cycling per IPC TM-650 2.6.7.2 in the same test chamber with one set-up. Via net resistance measurements are continuously monitored with one reading taken per net every second.

Both the IPC PCQR² and the IPC-6012 QML programs utilize the OM system test methodology. The PCQR² program provides strong statistical data that quantifies process capability, quality and reliability while the QML program is a sampling plan which verifies conformance to IPC specifications. We offer the OM Thermal Stress Systems for sale or lease, and test services are provided from both CAT and our service partners.

***Shaughnessy:** Thanks for your time, David.*

Wolf: Thank you. **PCBDESIGN**

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Hey, They're Just Vias—or Are They?

by Mark Thompson, C.I.D.
PROTOTRON CIRCUITS

From their traditional use to more unconventional uses, the via has gone through some changes over the years. In this month's column, I will examine issues such as:

- Expressing tolerances for vias
- Blind and buried vias
- When, where, and why you should fill vias
- Via-in-pad
- Stacked vias
- Vias for thermal applications

Expressing Via Tolerances on a Drill Drawing

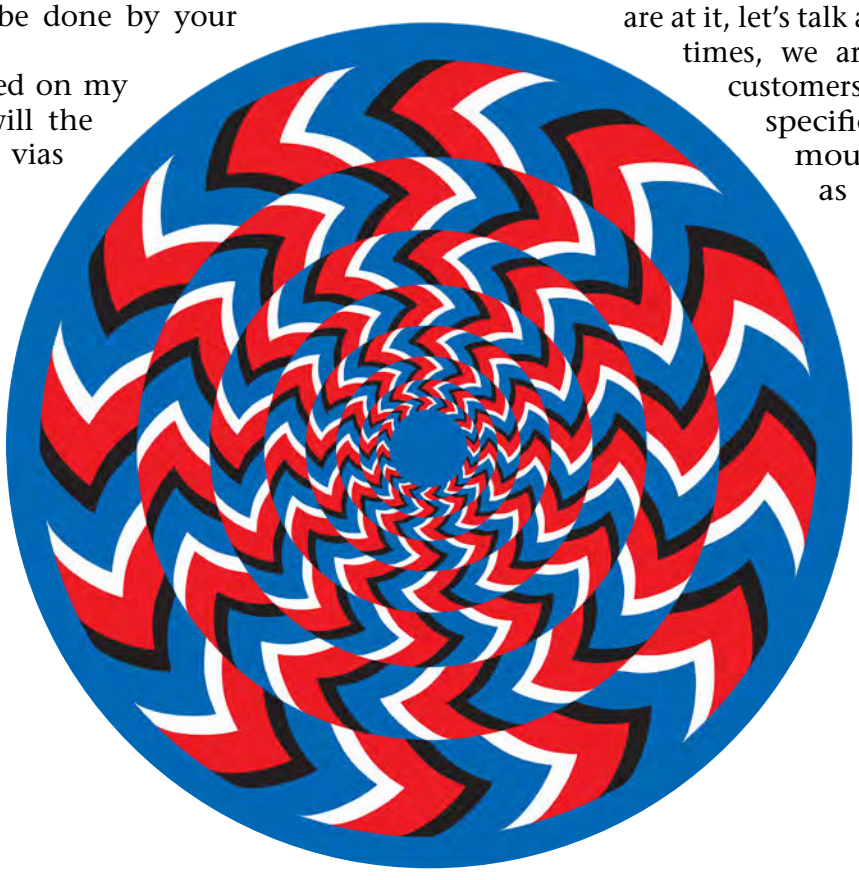
I get this phone call at least once a week: "Hey, Mark, what is the smallest mechanical via that can be done by your company?"

This is followed on my end by, "What will the tolerance for the vias in question be?"

If they say, "Oh, your standard +/-.003" tolerances," I am obligated to tell them the min via would be around .0078" with a signal pad of at least .014" and an anti-pad of at least .018". Usually, at this point I hear a lot of choking and coughing and they say, "But I am egressing from a .4mm pitch BGA, I don't have that kind of room!"

This is where we talk tolerance. If they are true vias where the finished size is NOT of any consequence, we say, "Why not call them out as +.003" minus the entire hole size?"

At that point I tell them that we can drill smaller and require less signal pad and anti-pad size, which opens the customer up for some routing for these fine-pitch parts. While we are at it, let's talk about pitch. Many times, we are approached by customers talking about a specific pitch between mounts or pads, such as .4mm or .5mm



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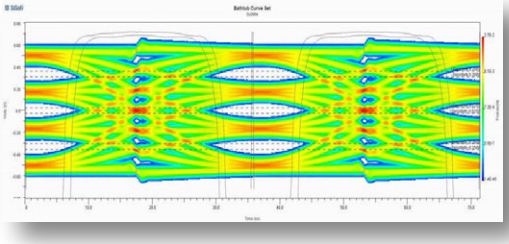

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pitch. Understand that without a design to see the via image data, it is difficult for a fabricator to properly understand what pitch means to the customer.

The pitch is the distance from the center of a given entity to the center of an adjacent entity. This can mean different things based on pad/mount size. Let me give you an SMT pad as an example:

A .5mm pitch means .0197" between the centers of two BGA pads or surface mounts. This seems like a very reasonable distance, given today's circuit board geometries. However, what if the designed surface mount pad width is .015" wide? This would mean a .5mm pitch would leave only .0047" edge to edge between the mounts. This gives you little or no room to route a trace between mounts at that width and pitch.

Clearly as the pitch between parts decreases based on today's shrinking chip footprints, the associated surface mount or BGA pad widths need to decrease as well to be able to route even a .003" or .004" trace between them.

Blind and Buried Vias

What exactly is a blind via? And what is a buried via?

Typically used when real estate becomes an issue and you have a finite amount of space to get all the interconnects done, a blind via goes from a given surface layer (top or bottom, or both) down to a specific layer. As an example, a blind via scenario on an 8-layer board may be blind vias on layers 1-2 and 7-8 and through hole. This is common for folks who want the best of both analog and digital in their designs; they may, for instance, have blinds on layers 1-2 and 7-8 in this scenario as Rogers materials to take advantage of very specific Dk and Df numbers for co-planar waveguides and then have all their less critical signals internally on a standard hi-temp FR-4 type.

A buried via is a via on a layer set internally that does not go to the surface. An example would be a 10-layer board with buried vias on layers 3-8.

This scenario would typically be constructed as a core cap, with core material between layers 1-2, 3-4,5-6,7-8 and 9-10. The layers 3-4,5-6 and 7-8 would then be laminated together forming the buried drill scenario. They would then be drilled as 3-8, imaged, plated, stripped, etc., and then laminated to the 1-2 and 9-10 in a final lamination process. The part is then through-hole drilled and finished as a standard multilayer.

The advantage of blind and buried vias is that of space. When all desired interconnects are exhausted by through-hole, you look at going to blind or buried vias to open routing space.

What do you need to know about them from a fabrication standpoint? It's straightforward, really.

Provide a separate NC drill file for each blind and buried via scenario. Optimally, provide separate drill drawings for the blinds or at least an additional table showing all drill scenarios in your drill drawing showing any blind or buried vias.

Remember than on a plane or split plane used as a blind termination layer, you must add pads to facilitate through-hole plating of the blind and/or buried section.

Many blind via scenarios assume some percentage of epoxy fill through the lamination process. To avoid surface dimpling from blind vias, many times customers specify an additional epoxy fill after lamination to maintain good surface flatness.

Which brings me to...

When should you specify via fill, and what type should you specify?

Why should you fill a given via with either epoxy or metal epoxy? First, let's talk about epoxy vs. a metal epoxy and why you would choose one over the other.

What is the obvious difference between the two? Well, the partially metalized epoxy fill is conductive. So a via that is designed with a thermal application in mind (for instance, to disperse heat from one side to the other) could benefit from metal epoxy, as opposed to epoxy fill that is non-conductive.

Remembering that the via itself will have plating in its barrel so there is still continuity regardless of whether it is filled with conductive or non- conductive type epoxy paste.

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Years ago, before epoxy and conductive epoxy were more prevalent, fabricators attempted to fill vias with mask material. This presented a problem at fabrication for BGA applications where you have a clearance for the via on one side but no clearance on the opposing side. With today's polymer plastic masks, this forms a plastic "cup" which does not allow the solution to move freely through the via when metallized and sometimes results in oxidation, creating electrical anomalies.

Today, for those same vias, or for via-in-pad, we can fill them with epoxy, planarize them (which is to say, make them flat) and flash plate over them, making the whole conversation about the absence of a clearance on one side or the other a moot point.

So, where else might I choose to fill a via? Some applications for filled vias are under chips and have stitching vias under them to dissipate heat.

Here again, the desire is to have a large metal land area on one side directly under the chip and nothing on the opposing side. This is another great opportunity for an epoxy or even conductive epoxy fill. See Figure 1.

In some applications, you may choose a conductive filled via for thermal applications to dissipate heat, such as a Faraday shield (Figure 2).

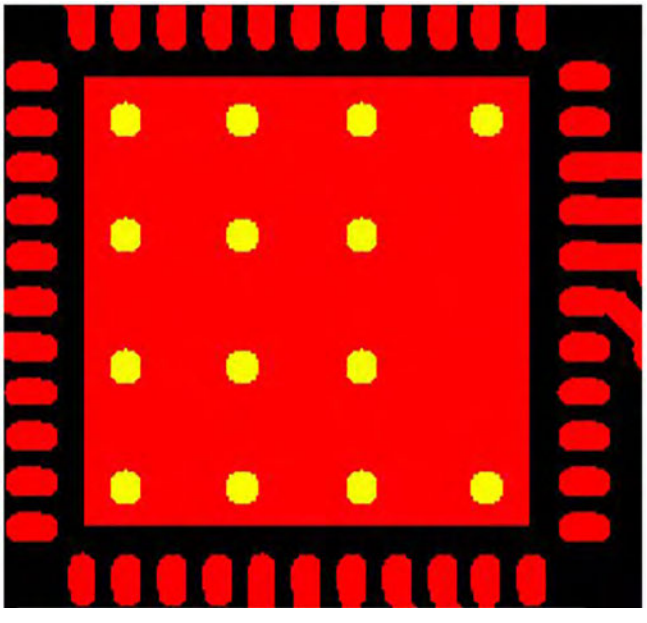

Figure 1: Vias stitched in a metal land.

In others, you may be more concerned with EMI and fill vias in the region of a ground strap (Figure 3).

And yet in other applications you may choose to stitch the vias on either side of an impedance controlled structure (Figure 4).

Via-in-Pad

Lastly, let's talk board geometry and when to epoxy fill via-in-pad applications, specifically where you do not have room to dog bone off a SMT and have a via in the SMT pad or partially in the SMT pad. These are also perfect situations where epoxy fill is advised. This way the via is plated, filled, made flat and encapsulated with more plating, the fact one side is exposed based on via-in-pad and the opposite side is walled off with mask is of no consequence for flatness, oxidation or dimples.

Laser and Stacked Via Structures

So, what happens when even you still do not have enough room for all the routing you may need, even when using blind or buried vias? You consider using laser drills or stacked vias.

The obvious benefit for a laser drill is size. If, based on geometries, you are relegated to a sub

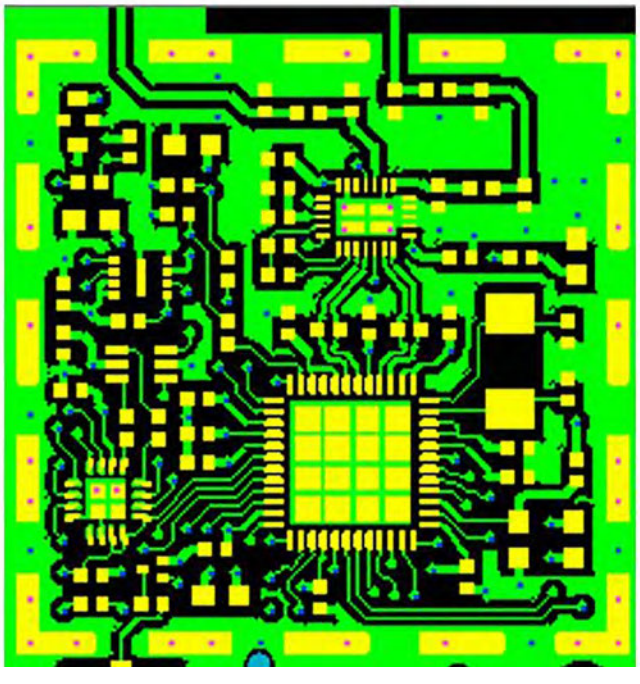

Figure 2: A Faraday shield with stitching vias.

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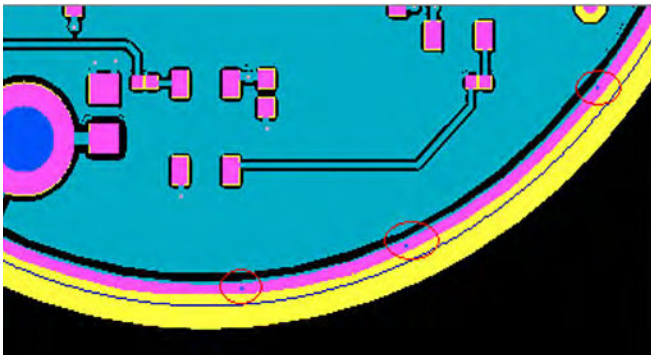


Figure 3: Stitching vias in a ground strap.

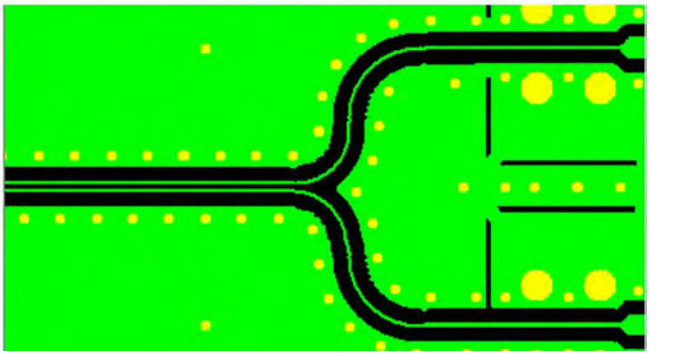


Figure 4: Vias stitched on either side of an impedance-controlled structure may provide better signal integrity and EMC.

.004" hole, you will need to look at laser drilling. The laser-drilled hole uses the pad and capture pad to register so these very fine laser holes typically have excellent registration, an obvious benefit for very dense parts.

Stacked vias are, as the name suggests, layer formations of very thin substrates with vias directly on top of each another. They typically are only used when board real estate is at a premium. Clearly the via is an ever-changing multifunctional structure. I have barely scratched the surface of the various uses of vias.

Note from a Fab standpoint on a Common Drawing Note

A common drawing note involves adding teardrops to all via terminations. A teardrop is added where the trace intersects the pad, in an effort to mitigate any misregistration of the via at the trace/pad intersect area.

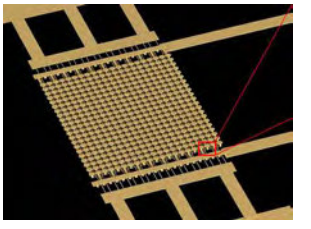
The problem is that vias are typically not on any specific grid and are sometimes placed very close to other metal features, making "teardropping" difficult and sometimes not possible without creating further gap issues.

I have enjoyed discussing the various uses of vias this month, and I hope you all learned a few useful tricks that will help you the next time you face a via problem. I will write another column on vias in the not-too-distant future.

As always, I appreciate your time. If you have any questions or comments, feel free to contact me. **PCBDESIGN**

Mark Thompson is in CAM support at Prototron Circuits.

Semiconductor-free Microelectronics Are Now Possible, Thanks to Metamaterials



Engineers at the University of California San Diego have fabricated the first semiconductor-free, optically-controlled microelectronic device. A team of researchers in the Applied Electromagnetics Group led by electrical engineering professor Dan Sievenpiper at UC San Diego sought to remove roadblocks to conductivity by replacing semiconductors with free electrons in space. However, liberating electrons from materials is challenging.

"Next we need to understand how far these devices can be scaled and the limits of their performance," Sievenpiper said. The team is also exploring other applications for this technology besides electronics, such as photochemistry, photocatalysis, enabling new kinds of photovoltaic devices or environmental applications.

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Vias, Modelling, and Signal Integrity

by Martyn Gaudion
POLAR INSTRUMENTS

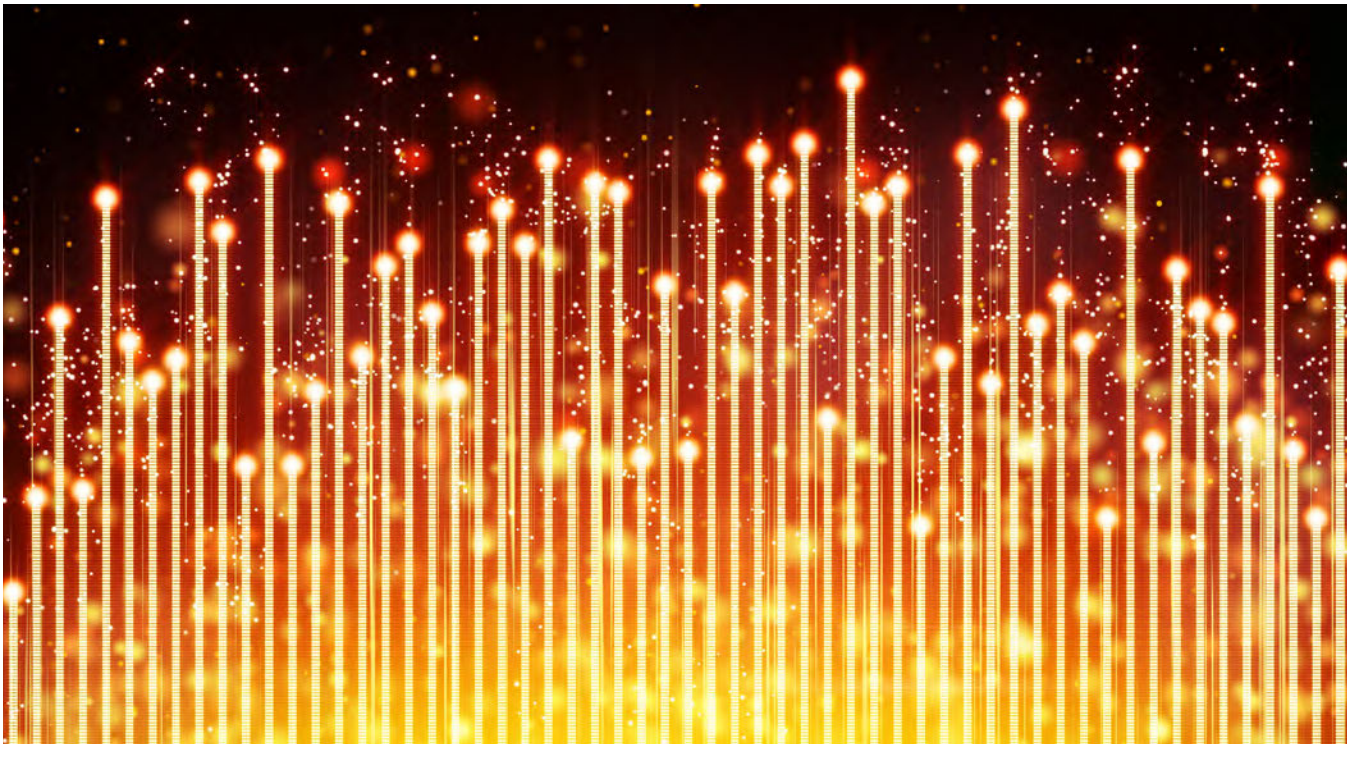
Editor Andy Shaughnessy recently sprung a request on me: Would I like to write an item on vias? A complex and tricky subject, I thought. But after some reflection it seemed like a good idea…so, here goes.

I was just about to leave for PCB West in September, and my connecting flight developed a fault. Always better when the plane breaks on the ground than in the air, but inconvenient nevertheless. If you want to be certain to catch your long-haul flight, says the ground agent, you must go via London Gatwick.

I'll cut a long story short, but I had 10 minutes to decide. Should I, on the one hand, get to London Heathrow via London Gatwick, or take my original connection which maybe will, maybe won't, get me to Heathrow in time for my connection? I bit the bullet, had my bags offloaded and started the process of looping through security and booking a new flight on an alternate airline only 45 minutes before departure whilst at the same time trying to book an overnight hotel whilst going through security to the new flight.

In the process, I became one of those annoying people who is on the phone at the gate and up the jetway. I did try to book online but that's a mare too when you are in a rush. Still, I got the last room available close to the desired terminal.

What's all that got to do signal integrity? Well, it's a lot easier to go somewhere by a direct route than via somewhere else. The same is true for signals. The best a designer can do is to ensure the via offers the least inconvenience to the signal; otherwise it's going to end up at its destination a bit grumpy and battered out of shape, just like I was when I boarded the aircraft for the long-haul flight the following morning. Though



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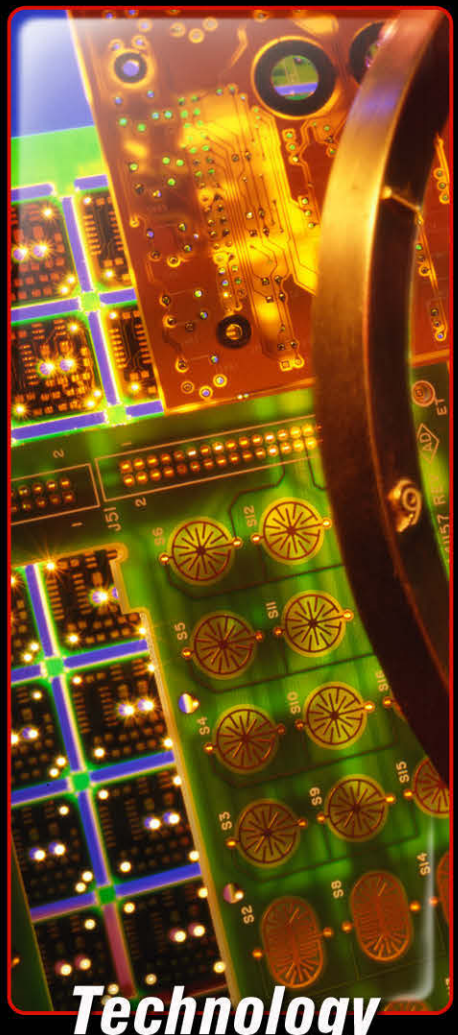
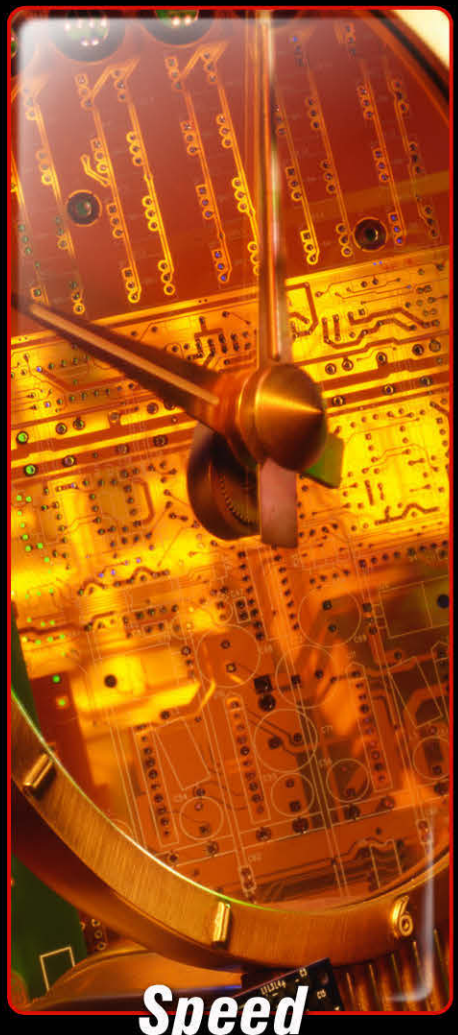


Technology



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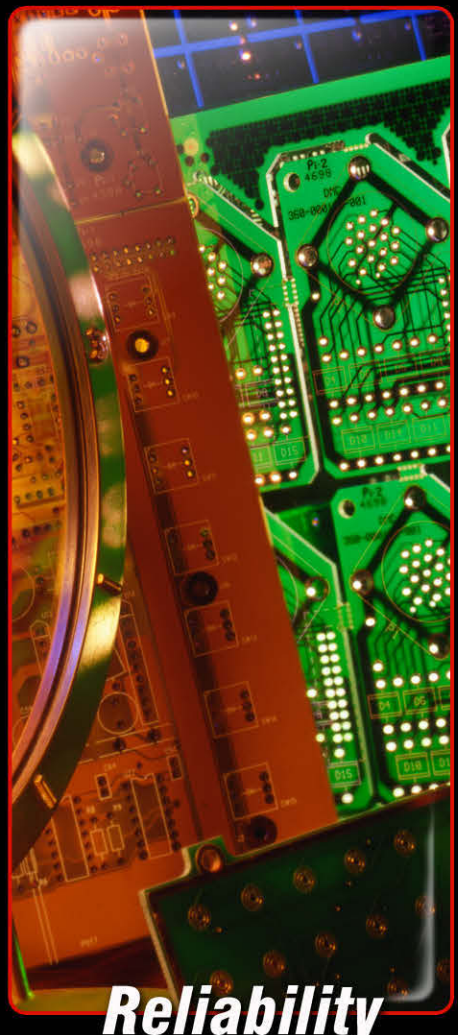

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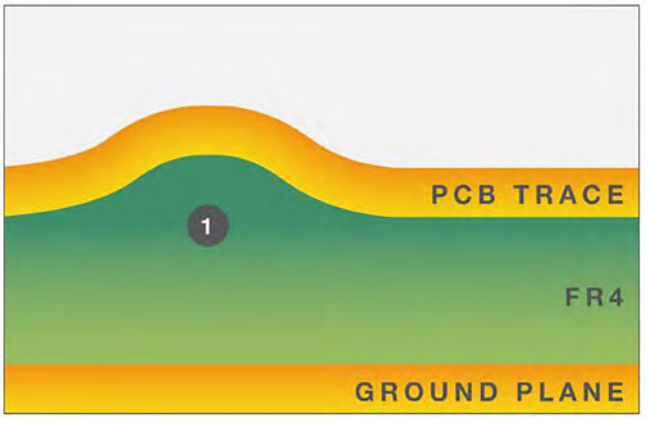

Figure 1: An imagined view of pulse "stretching" the dielectric. The numeral 1 denotes stored energy.

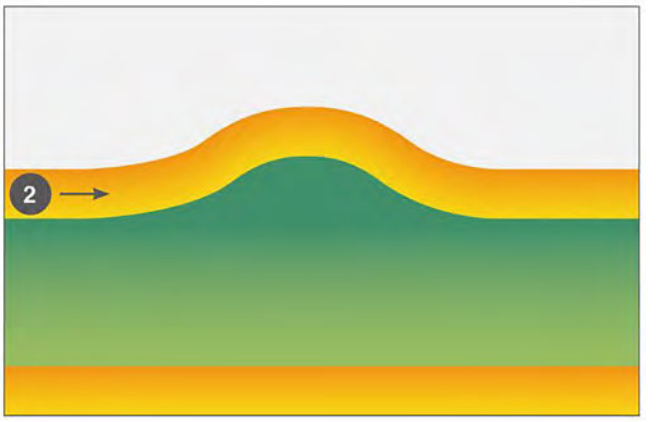

Figure 2: The energy propagates along the line. The numeral 2 denotes the direction of the current.

a few glasses of shiraz later, my mental state had equalised. But signals aren't always so lucky.

Before delving down into the electrical via, I would like you to have a think about the following scenario on a transmission line. Bear with me: Understanding the following will help make more sense of the via scenario. The second thing I would like you to bear in mind simultaneously is that good modeling can't fix a bad design. The model can tell you where a design is weak, but if you have committed your design to product, the model can only tell you how it behaves. Some less experienced designers seem to fall into the trap of thinking a better model will fix something that doesn't work; it won't. It will only reassure you that the design was bad in the first place.

But back to the simple transmission line. Let's take a microstrip for example; it has a surface line running over a return path. So, in a mind experiment, let's put two major failings on this imaginary (let's say, 5 inches in length) microstrip. Remember also that when you excite a transmission line with a signal, the signal propagates down the line at roughly half the speed of light (a bit more in a microstrip). In our imaginary microstrip, I'd like you to imagine you have cut out a slot in the ground plane about halfway along the trace and at right angles to it, for whatever reason. What's going to happen to your transmission line?

As the signal propagates along the trace, everything is normal—an equal and opposite current returns to the source in the ground plane immediately under the outbound signal. In front of the signal the line is quiet. Nothing is outbound (it hasn't gotten there yet) and no return; there's nothing to return. When the signal traverses the slot, well, everything gets messed up as there is no immediate return path. You have just created a slot antenna and the current attempts to find the path of least impedance back to the source (which might be in the air). This is poor design, but I still see it happen from time to time. To imagine just how ridiculous this is, let's swap the scenario, making the ground continuous but at halfway along the surface trace, we have an open circuit for half an inch. "That will never work," I can hear you say. "It's an open circuit!" But in this scenario, some less experienced designers were happy to put an RF open circuit in the return by cutting an aperture below the outbound trace.

Here is my visualisation of a side view of the transmission line. With an overdose of interpretation, I have imagined that the signal energy is stored in the substrate by stretching it like a piece of elastic. The signal propagates along the copper by storing energy in this imaginary medium by stretching the molecules so it expands… clearly some fantasy is involved here, but it should help you visualise the signal wavefront travelling through the transmission line, and what happens when the return path is disrupted.

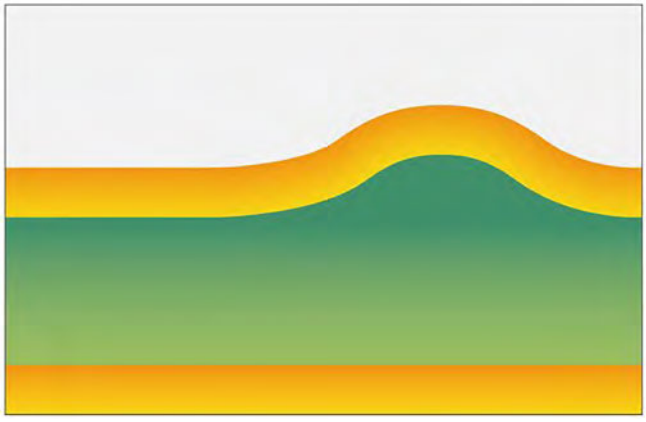

Figure 3: Energy continues to propagate until…

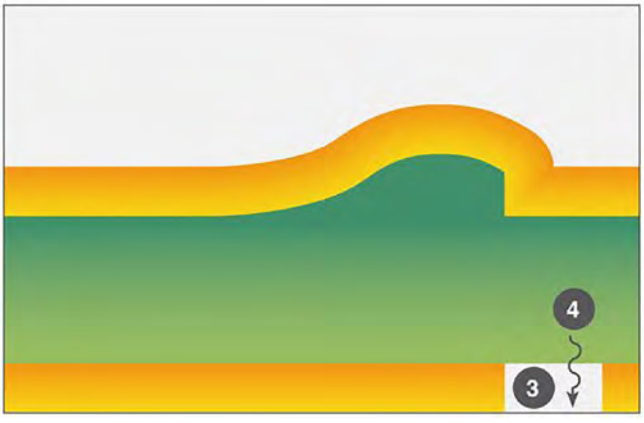

Figure 4: …Until meeting a slot in the return path (3), which causes energy to radiate (4).

Now, back to vias. I always like to look at subjects in an alternate way, as presenting the information in an unconventional method forces you to think a little more. In this case, the thoughts should become easier. Imagine for a start that the board is not 63 mils thick, but 6 inches thick. Then turn the board vertically in your mind so you send the signal "along" your imaginary via. What does it experience?

Well, whilst the signal path may be a cylinder (or maybe a cylinder with fins if you have left non-functional pads on the via) and be a reasonable outbound path, the return path for a single-ended via is far from straightforward. The now horizontal (in your mind) via will traverse over a series of power and ground plane edges interspersed with insulators. What on earth is the return current going to do now?

Think back to the simple microstrip example where I posed the question of a slot in the plane: it forms a slot antenna. The same is true here, and there are as many slot antennae as signal/

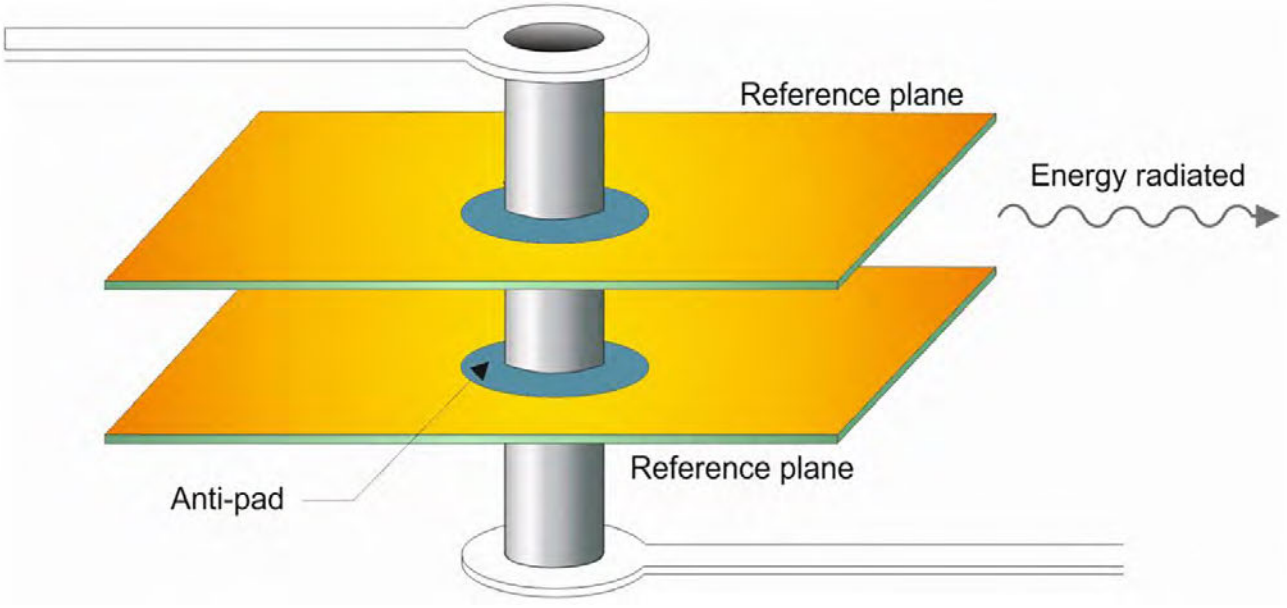

Figure 5: Without a return via the return current will attempt to radiate between the planes.

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ground plane pairs; as a result, the return current on a badly designed single-ended via finds itself trying to radiate out through each plane pair and radiates until it meets a boundary; often, this is the open circuit at the edge of the board. Needless to say, this is a very complex 3D scenario to model. However, all is not lost. Recall my note at the start that modelling can't fix a poor design. So, how do you mitigate the effects of vias? There are several approaches, depending on how demanding the application is, and only once you have thought of an appropriate approach does it make sense to start modeling to confirm your design.

"There are several approaches, depending on how demanding the application is, and only once you have thought of an appropriate approach does it make sense to start modeling to confirm your design."

A first step would be to keep the via as short as possible by using microvias or blind or buried vias. Second, you should consider the challenge of via stubs: if a trace goes from L1 to L3 but leaves a stub down to L16, the signal will traverse though all the layers to L16 before reflecting to L3, giving an effective electrical stub length almost double the mechanical one. In the case of very thick boards with through-hole vias, back-drilling is an option to remove the unnecessary part of the via barrel. However, another approach is maybe a little counter intuitive: It may be better to run the signal down the full depth of the via and back up an adjacent via to reach the desired layer, as this could present a shorter stub than just going down one layer and leaving a long stub.

Going back a moment to the explanation of the challenging return path seen by the return current from a single via, you can make life easier for the return current if you design a return path rather than leaving it to chance. So, by adding a return via adjacent to the signal via you give the return current a favourable path back to the source rather than allowing the high frequency to bounce around in the cavity between the planes.

This also leads to one of the reasons that differential transmission is popular for high-speed signals: Aside from its inherent noise immunity, the balanced differential pair means you provide an outbound AND return path in the signal via pairs without having to think about it. In other words, the signal integrity of a differential pair is inherently less effected by transition through vias than for the single ended case.

As always in *The Pulse* columns, I have avoided too much in-depth analysis. I've rather given some guidance to help you get a better feel for the behavior of vias. I hope that you consider these points, so that when you do come to design high-speed vias, you'll have a head start. When modelling is required, now you'll know that you should not expect a good model to fix a bad design.

Instead, you can use modelling to confirm your design, which has started from a good perspective. In many cases, you can attempt to keep the geometries small enough that the via is invisible. (*Shameless plug:* The via stub length indicator in the Polar Si9000e PCB transmission line field solver can help.)

One closing thought. Wouldn't it be great if an HDI wizard could create a coaxial via so the high-speed signal didn't see all those nasty slots between planes as it traverses down through the board? Well it has been done, and patented; an online search will show you some of the ideas. I imagine it is not as easy as it seems, or it would be a mainstream approach by now. I would love to hear back from fabricators on this topic.

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Martyn Gaudion is CEO of Polar Instruments. To contact him or view past columns, click here.

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PCB007 Highlights

Weiner's World

This month, I was a guest at the High Density Packaging Users Group (HDPUG) meeting in Nashville, Tennessee. The consortium, composed of more than 50 companies (small and large) in the electronics packaging supply chain, conducts projects to solve real world problems or develop data for product parameters, package/component life, and production processing.

ECWC14 Seeking Abstracts for 14th Electronic Circuits World Convention

The 14th Electronic Circuits World Convention (ECWC14) will be held in KINTEX, Goyang City, South Korea from April 25–27, 2017 along with the KPCA Show hosted by Korea Printed Circuits Association (KPCA) and the World Electronic Circuits Council (WECC).

Volunteers Honored for Contributions to IPC and Electronics Industry

IPC—Association Connecting Electronics Industries presented Committee Leadership, Special Recognition and Distinguished Committee Service Awards on September 26 at IPC's Fall Standards Development Committee Meetings in Rosemont, Illinois.

Lessons in Leadership From My Father

When I was asked to contribute an article for this issue on leadership, I thought it was an opportune time since my Dad, Nagji Sutariya, had recently passed away. I had spent nearly every daylight hour with him since I started working with him at Saturn in 2001.

Happy's Essential Skills: Recruiting and Interviewing

Hopefully, your career has progressed to the point that you are empowered to recruit your own team or a key person for your team. There are always technical people looking for better jobs, but many times, the most talented are busy doing their work and not looking for a new opportunity.

Institute of Circuit Technology Hayling Island Seminar 2016

In recent years, the Hayling Island Seminar has become established as the most popular date on the Institute of Circuit Technology calendar and, as expected, the 2016 event attracted a large gathering of industry professionals to the south coast of England to share knowledge and experience.

Ventec Talks Strategies to Gain Market Share

At electronica 2016 in Munich, Germany, Tamara den Daas, OEM global account manager at Ventec International Group, speaks with I-Connect007's Pete Starkey about Ventec Europe's 10th anniversary, as well as the relevance of electronica for the company.

Mayim Bialik Chosen as Opening Keynote at IPC APEX EXPO 2017

Actress and neuroscientist Mayim Bialik has been selected through a vote of electronics industry professionals to present the opening keynote at IPC APEX EXPO on Tuesday, February 14, 2017 in San Diego.

Happy's Essential Skills: Metrics and Dimensional Analysis

After 20 of my columns, readers probably realize that I am an analytical person. Thus, I dedicate this column to metrics—the method of measuring something. I mentioned the four levels of metrics in my June column "Producibility and Other Figures of Merit." I also introduced the five stages of metrics in the second part of the column "Design for Manufacturing and Assembly, Part 2."

A New Facility in India for PCB Fabricator ACI

I-Connect007's Barry Matties met with Raj Dhanani and Bryan Ricke of Advanced Circuitry International to discuss their growing footprint in India, recent investments in their U.S. facility, and the future of the RF and antenna markets.

Uncommon Sense

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

When common sense fails, tap into your uncommon sense. While common sense is considered conventional wisdom, uncommon sense is a re-examination of that conventional wisdom. Basically, common sense teaches us that the way it has always been done is the right way, and that's just how things are. Following common sense is usually the safe way to go. But the people who are really making a difference in the world are usually the people who try something new. Tapping into our uncommon sense allows us to take a deeper look at things we often take for granted.

It is remarkable that with all of today's high-performance systems, in which very complicated electromagnetic effects play a dominant role, many of us still hold misconceptions about the fundamental nature of how signals interact with interconnects. In this month's column, I will look at the contemporary ways of addressing an old issue (déjà view, as I call it) and go beyond the design of PCBs.

There is always a debate regarding how a differential pair should be routed. Conventional wisdom tells us that since the two halves of the pair carry equal and opposite signals, a good ground connection is not required as the return current flows in the opposite signal. And tight coupling between the signals is better than loose coupling as it reduces undesirable coupling/crosstalk from aggressor signals. And let's face it, it is easier to route a pair together so that we logical manage the planes, aggressor signals and matched delay simultaneously particularly in complex designs.

Some argue that beyond the fact that differential pairs transfer equal and opposite signals, there are no special requirements that need to be considered when using differential pairs. They should be treated as two single ended signals. The signals of a differential pair don't need to be routed together, should not be tightly coupled and are not required to be routed to the differential impedance.

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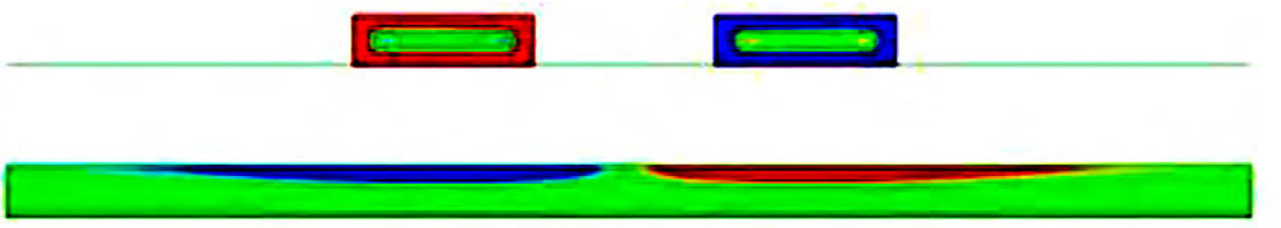

Figure 1: Return current paths of a differential pair (courtesy Ansoft).

Basically, a differential pair is two complementary transmission lines that transfer equal and opposite signals down their length. We assume that tightly coupled differential pairs have no current in the adjacent planes because the return current of one line is carried by the other. That is not correct. On a PCB, the return current path, of each trace of the pair, flows directly below each trace in the reference plane as seen in Figure 1.

If the differential pair is well balanced, then tight coupling will achieve an effective degree of field cancellation. However, if they are not perfectly balanced, then the degree of cancellation is not determined by the spacing, but rather by the common-mode balance of the differential pair. Most digital drivers have poor common-mode balance and therefore differential pairs often radiate far more power in the common-mode than in the differential-mode. In such a case, one gains no radiation benefit from coupling the differential traces more closely together.

According to the FCC Class B compliancy standard, the differential-mode radiation from a microstrip pair, with 20mil separation, should theoretically yield a 40dB radiation improvement at 1 GHz over the radiation one would measure from the same signal routed as a single ended trace. It is the common-mode signal that dominates the radiation and decreasing the pair spacing will not improve this situation.

For a perfectly balanced differential signal, the radiation from one trace exactly cancels the radiation from the other as they are equal and opposite. However, a common-mode signal represents an average of the two signals in a pair. The radiation is identical on both traces and therefore it does not cancel but rather reinforces. To minimize radiation and crosstalk you must think explicitly about the common-mode component of the differential signal—skew creates this common-mode signal.

Arguably, the principal source of imbalance is time delay skew between the two traces. The easiest way to minimize this skew is to match the electrical lengths and to correct any shift immediately, after it arises, by adding length (hence delay) to the shorter trace. Unfortunately, time-delay skew can also be introduced by a variation in the dielectric constant of the glass-resin composite. This, weave induced skew, can be minimized by using materials with a spread-glass weave such as the new Isola I-Speed, I-Speed IS and Tachyon-100G that have been specifically developed for high-speed applications.

The transformation from differential to common-mode also takes place on bends and non-symmetrical routing near via and pin obstructions. In a previous column, Beyond Design: Differential Pair Routing, I concluded that symmetry is the key to successfully deploying differential signals in high-speed designs. Maintaining the equal and opposite amplitude and timing relationship is the principle concept when using differential pairs. Mirror symmetry (as in Figure 2) about an axis, along the interconnects, avoids mode transformation. The symmetry property preserves the signal in the differential-mode which does not radiate. Common-mode noise may have little effect on signal integrity, but will have a more serious impact for EMI.

Mode transformation can also be minimized by reducing the size of any bends in the pair. Any skew introduced, by a bend, should be corrected immediately after the bend so that the majority of the length of the pair is balanced. Also, routing in a stripline configuration has

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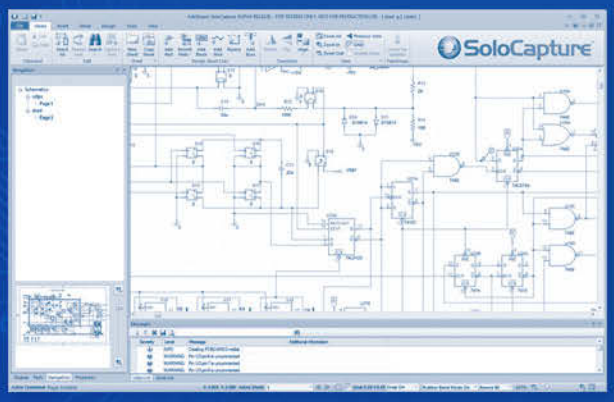

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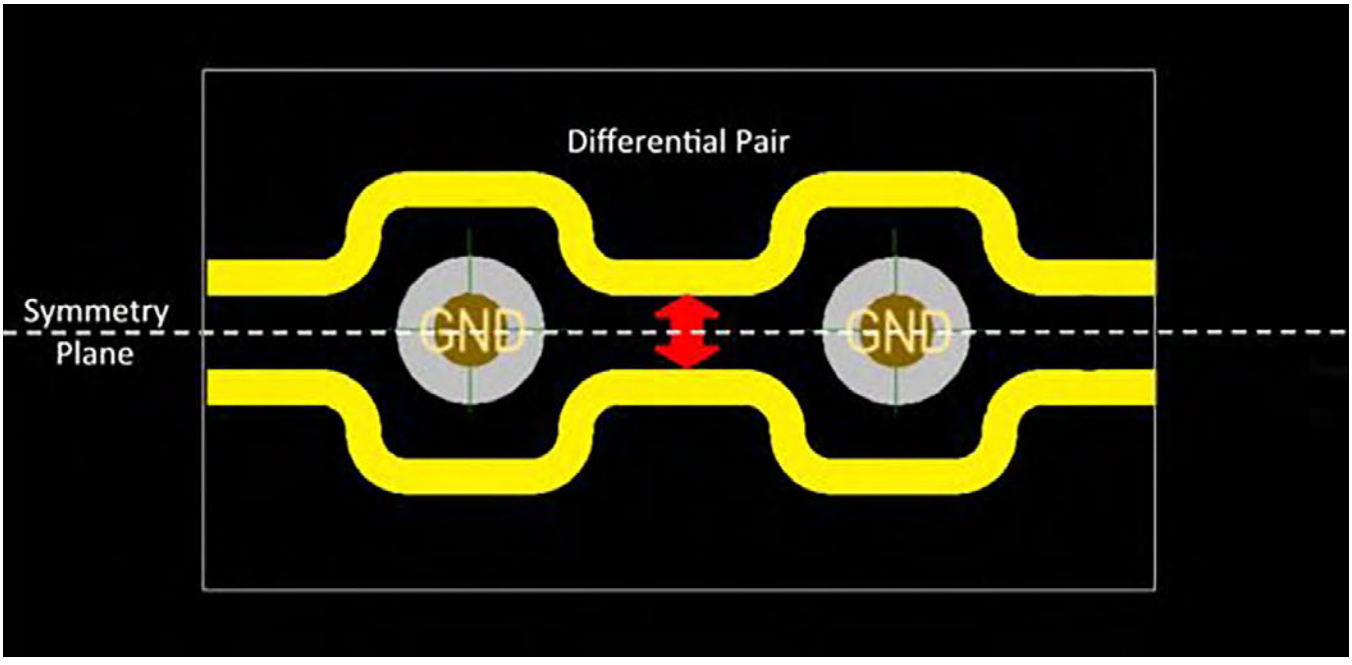

Figure 2: Differential pair symmetry.

equal common and differential-mode propagation velocity which helps reduce far end mode transformation.

It can be seen in Figure 3, that the differential impedance of this particular microstrip pair, levels-off at 100 ohms above 12mils trace clearance (blue curve). This is simulated quickly by multiple passes of the field solver. So, all other factors being equal, the differential impedance will always be 100 ohms regardless of increased spacing. This allows the pair to be split to traverse obstacles (vias or pins) without altering impedance. This curve provides a clear map of the design space and can increase your productivity by efficiently defining the stackup configuration for single ended and differential pairs. In this case, once the separation is greater than 12 mils, the two traces convey single ended signals.

A few signaling standards have both differential and common-mode impedances specified, but many do not. This provides the freedom for the user to set it according to their application. These two impedances are related to the coupling strength of the differential pair. As the traces get closer, both differential and common-mode impedances are reduced.

With loose coupling, there is always the case where the traces must be bought closer

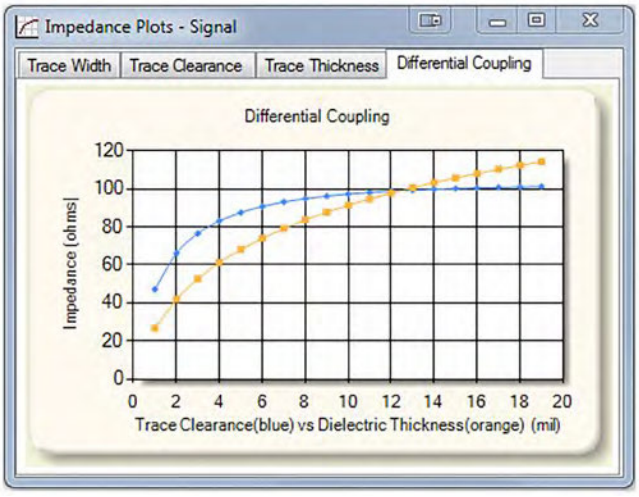

Figure 3: Differential impedance levels-off above 12 mils, simulated by the iCD Stackup Planner.

together to weave through constrictions such as connector fields, BGA balls, vias and other land patterns. As the traces are bought closer together the impedance drops, so the traces must be made narrower to compensate. The majority of PCB fab shops limit the trace width to 3 mil minimum. And of course, the narrower the trace width; the more the expense.

Also because of the narrower traces, the

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current is forced into a small width of copper. This increases trace resistance, inductance and skin-effect losses. Contrary to common belief, closely coupled pairs do not improve EMI. This is because it is the common-mode signals from the drivers—the natural imbalance (skew)—that radiates.

In conclusion, to minimize radiation and crosstalk, of a differential pair, one must think explicitly about the common-mode component of the signal. It is not a matter of which is better—tight or loose coupling—but rather which scenario better avoids timing skew that creates this common-mode signal. It is imperative to determine exactly where the differential impedance levels-off. But without a good field solver that simulates signal coupling and flight time, you are really just taking a stab in the dark, which is not good design practice.

Points to Remember

- Conventional wisdom tells us that tight coupling between the signals is better than loose coupling, as it reduces undesirable coupling/crosstalk from aggressor signals.
- On a PCB, the return current path of each trace of the pair flows directly below each trace in the reference plane.
- If a differential pair is not perfectly balanced, then the degree of cancellation is not determined by the spacing, but rather by the common-mode balance.
- Most digital drivers have poor common-mode balance and therefore differential pairs often radiate far more power in the common-mode than in the differential-mode.
- For a perfectly balanced differential signal, the radiation from one trace exactly cancels the radiation from the other as they are equal and opposite.
- The common-mode signal represents an average of the two signals in a pair. The radiation is identical on both traces and therefore it does not cancel but rather reinforces.
- To minimize radiation and crosstalk, you must think explicitly about the common-mode component of the differential signal—skew creates this common-mode signal.
- To minimize the skew, match the electrical lengths and correct any shift immediately, after it arises, by adding length (hence delay) to the shorter trace.
- Time-delay skew can also be introduced by a variation in the dielectric constant of the glass-resin composite.
- The transformation from differential to common-mode also takes place on bends and non-symmetrical routing near via and pin obstructions.
- Mirror symmetry, about an axis along the interconnects, avoids mode transformation. The symmetry property preserves the signal in the differential-mode which does not radiate.
- The differential impedance of a pair, levels-off at a particular coupling point. Beyond this point, the differential impedance will always be the same regardless of increased spacing.
- As the traces get closer, both differential and common-mode impedances are reduced so the traces must be made narrower to compensate.
- Narrow traces increase trace resistance, inductance and skin-effect losses.
- Contrary to common belief, closely coupled pairs do not improve EMI. **PCBDESIGN**

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1. Barry Olney, Beyond Design, "Differential Pair Routing."
2. Eric Bogatin, Fundamental Myth-Conceptions.
3. Lee Ritchey, Right the First Time.
4. Yuriy Shlepnev, Analysis of differential line transition from tight to loose coupling, and practical notes on mixed-mode transformations in differential interconnects.
5. Howard Johnson, High Speed Digital Design.

Barry Olney is Managing Director of In-Circuit Design Pty Ltd (iCD), Australia. The company is a PCB design service bureau that specializes in board-level simulation. iCD developed the iCD Stackup Planner and iCD PDN Planner software. Visit www.icd.com.au

MilAero007 Highlights

All About Flex: Flex Circuit Specifications for Commercial and Military Applications
Applications across the various markets for printed circuit boards can have significantly different specifications and performance requirements. IPC-6013 is an industry-driven specification that defines the performance requirements and acceptance features for flexible printed circuit boards.

EIPC Reliability Workshop, Tamworth, UK, September 22, 2016
EIPC's reliability workshop, presented in cooperation with Amphenol Invotec, attracted a capacity audience from eight countries—some delegates having travelled from as far away as Russia—to take the opportunity to learn first-hand how to meet OEM, ODM and EMS product quality and safety requirements, and to understand how interconnection stress testing techniques could be applied to determine the reliability of multilayer PCBs.

The Right Approach: FOD and the Aerospace Industry
Unless you are currently building aerospace product to AS9100, you are probably saying, "What the heck is FOD?" What started out as a requirement to prevent damage to aircraft parts such as engines has been flowed down to any component or assembly including PCBs.

John Cardone on Designing Flex for Spacecraft
If you watched footage of the Mars rover driving all over the red planet, you're familiar with some of John Cardone's handiwork. He's been designing rigid, flex, and rigid-flex circuitry for spacecraft since he joined JPL in the early '80s, and he's worked on some of the more ground-breaking flex circuits along the way.

American Standard Circuits Achieves AS9100 Rev C Certification
American Standard Circuit has achieved its AS9100 Rev C certification, the internationally recognized quality management system standard specific to the aerospace, aviation and defense industries. This standard is strongly supported and adhered to by major aerospace OEMs and is being required by vendors within the supply chain on an increasing basis.

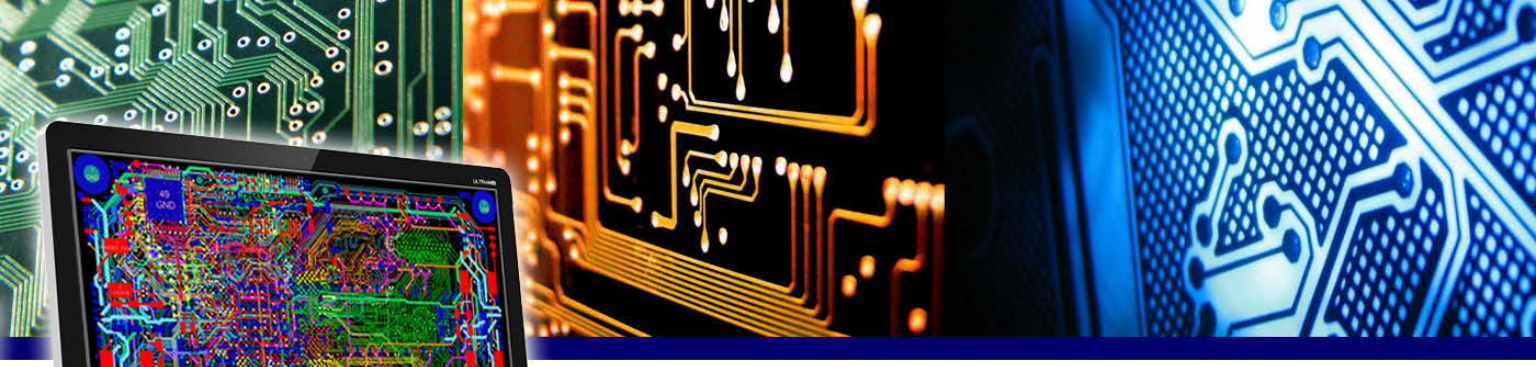
Eltek Has Supplied $1.6 Million Orders to a Strategic Customer
Eltek Ltd. announced today that since January 2016 it has supplied approximately US$ 1.6 million of technologically advanced solutions to a strategic customer. The customer selected Eltek because of its capability to produce high-performance and reliable solutions.

Flex Talk: Troubleshooting Flex Circuit Applications for Mil/Aero Projects
I imagine that everyone has been in this position at one time or another: Despite everyone's best attempt at creating the perfect design, PCB fabrication and assembly, something goes wrong and the troubleshooting begins.

Colonial Circuits: A Veteran-Owned Small Business
Mark Osborn, president and founder of Colonial Circuits, a truly American board shop specializing in the fabrication of high-technology PCBs, is also a proud Vietnam veteran who is still serving our country by building PCBs for most of America's critical defense and aerospace programs.

Cirexx Develops High-Heat Flex Circuits with HT Material
Cirexx International now offers a line of flexible circuit products that employ the recently developed DuPont Pyralux high-temperature HT material.

Flex Talk: Troubleshooting Flex Circuit Applications for Mil/Aero Projects
I imagine that everyone has been in this position at one time or another: Despite everyone's best attempt at creating the perfect design, PCB fabrication and assembly, something goes wrong and the troubleshooting begins.



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Resins: Five Essentials to Achieve the Right Cure

by Alistair Little
ELECTROLUBE

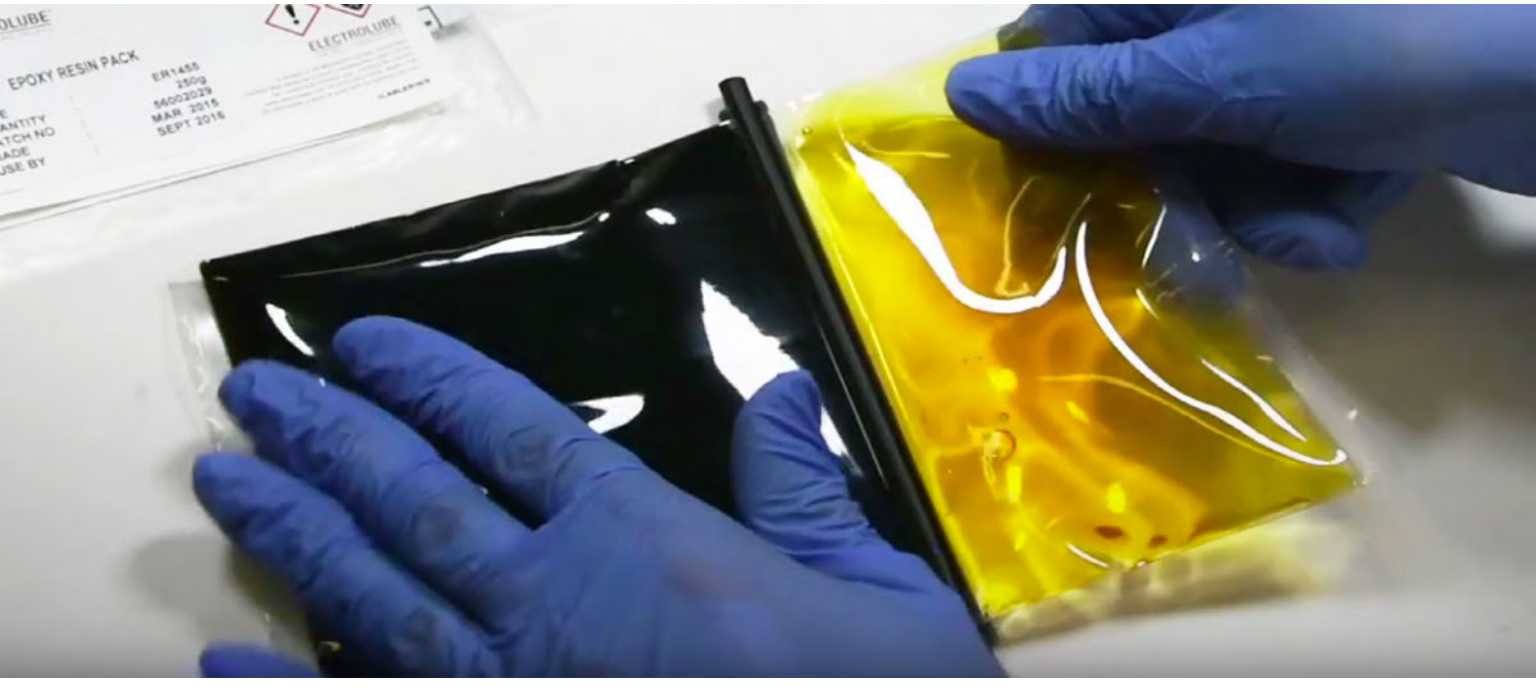
Last month, I looked at some of the critical things you need to consider before selecting your resin, which covered hardness, colour, viscosity and cure time. I do hope readers found this simple back-to-basics guide a useful starting point for further study and consultation. Of course, when it comes to the choice and application of resins, there's a lot of information to take in, and over the following months I hope to distil this and provide some useful tips and design advice that will help you in your quest for reliable circuit protection.

Right, you've now chosen your two-part resin and it's time to mix the components and get to work, so this month I'm going to turn my attention to the all-important job of mixing the resin (Part A, to use the terminology) and hardener (Part B), taking care that you get the ratio right and that you are conducting this critical part of the procedure under the right atmospheric conditions, and with all due regard for safety procedures. Get the mix wrong at this early stage and you will not achieve a satisfactory cure, which will ultimately lead to all sorts of problems later for the product you are potting or encapsulating. Anyway, continuing the five-point guide format that I introduced last month, here are five things to make yourself aware of before you start mixing.

Mix Ratio

Quite possibly the most critical aspect of resin mixing, which will have long term adverse repercussions if you get it wrong! There are two methods of mixing a resin with its associated hardener: by hand or using specialist dispensing equipment. If mixing by hand, then the ratio of the weight of the two components is the more useful method to employ. If mixing using dispensing equipment, then the volume ratio is used.

If the job is relatively small, then you are likely to use a resin pack, which provides the resin and hardener in precise quantities, in sep-



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arate compartments of the pack. When you are ready to use the product, you simply remove the clip or other separating device between the compartments and 'massage' the resulting pouch, ensuring that both components are completely mixed.

For larger production jobs, resin and hardener are likely be supplied in separate bulk containers and you will need to check the shot sizes for each component regularly to ensure that the correct amounts of resin and hardener are being dispensed and mixed correctly.

> "When mixing bulk resin and hardener, it is important to avoid introducing excessive amounts of air, which will form micro-bubbles within the cured resin."

When mixing bulk resin and hardener, it is important to avoid introducing excessive amounts of air, which will form micro-bubbles within the cured resin. These may expand with the temperature rise to such an extent that they may cause problems. Polyurethane resins are particularly sensitive to moisture, so humid air could also pose problems.

If you are not happy with bulk materials mixing and incurring the potential problems of introducing too much air (and moisture) into the mix, then it might be more appropriate to use automatic mixing equipment, which will accurately mix resin and hardener in the correct proportions, and usually in a controlled atmosphere.

Remember: Incorrect ratios will lead to a poor cure and the physical properties of the resin will differ from those specified in the manufacturer's data sheet.

Viscosity

As well as the viscosity of the mixed system, the viscosity of the two components needs to be considered. Often there is a large difference between the two components, particularly with filled systems, and this could place additional strain on the dispensing equipment's pumps and pistons. It should also be noted that viscosity of each component will vary depending upon the temperature of the environment in which the mixing and dispensing is taking place.

Usable Life/Gel Time

The useable life is defined as the time that the mixed resin can flow and is still workable; the gel time is the interval between mixing and the point at which the resin has just set and cannot flow. In the latter state, however, the resin is still relatively soft and can often be reshaped by applying slight pressure. Gel time is usually quoted for a sample size of 150g, and it is important to note that the larger the volume of mixed resin, the shorter the useable life and gel time. As a rule, all resins should be mixed and dispensed within their useable life. Fillers generally do not affect the gel time; however, gel time may be affected if the rate of cure or the cure reaction is influenced by fillers, so this should be ascertained if any minor working is required prior to the final cure.

Cure Temperature

Again, this is normally stated for a 150g sample size. Once a resin and its associated hardener are mixed together, the reaction can be very fast but also very exothermic, which can lead to the possibility of a runaway reaction. The exotherm temperature can be controlled by adjusting the volume or by using a filled system, as the fillers absorb some of the heat as well as reducing the concentration of the hardener that promotes this rapid cure. It should be noted that the temperature at which the resin is cured will affect not only the rate of cure, but also the development of cure. Controlling the cure temperature is important because the components requiring potting or encapsulation might be adversely affected by raised temperatures.

Although the volume of the resin applied is important, so is its depth and the surface area it covers. Every application is different, so resin users should take the curing temperature data

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provided in the manufacturer's data sheet as a guide to ensure optimum performance of their potting/encapsulation process.

Health and Safety

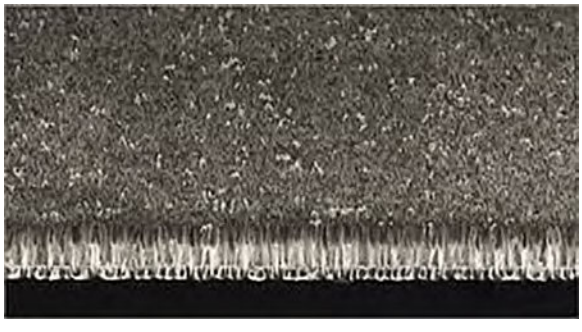
Resins are generally formulated to be as safe as possible during dispensing and mixing, and certainly safe when cured as part of the end-product. However, with the introduction of the Globally Harmonised System of Classification and Labelling of Chemicals (more succinctly: GHS), many of the hazards pertaining to resins have been re-assessed and resin chemists have been hard at work to develop safer and better performing resin systems. In any event, users should always study the relevant safety data sheets before using any resin product. In general, Part B (the hardener) is more hazardous than Part A (the resin). Good hygiene practice should always be followed, with gloves, eye protection and suitable clothing worn, and good ventilation/extraction available in the work area.

Well, hopefully the above advice will help get you started as far as resin mixing is concerned. Look out for next month's column, in which I will take a closer look at resin application and tricks of the trade to ensure a smoother application process and more effective cure. **PCBDESIGN**

Alistair Little is technical director for Electrolube's Resins Division.

Nanopillars: A State-of-the-Art Optical Sensor

Reliable, cheap and quick recognition of molecules at challenging concentrations of ~1 ppb (parts per billion) or less is now possible thanks to a sensor developed at DTU Nanotech.



Potential analytes include toxic food additives, chemical warfare agents, hazardous building materials and human disease markers.

The sensor consists of nanopillars with heights of 600 – 800 nm. These pillars are able to enhance significantly the spectroscopic fingerprints of the target molecules nearby, making them distinguishable at ultra-low concentrations. The technique is called surface-enhanced Raman spectroscopy (SERS).

Postdoc Kaiyu Wu from DTU Nanotech says that "an ideal sensor for SERS should exhibit reproducibly high enhancement over macroscopic areas and be cost effective. It is extremely difficult to fulfil both."

The nanopillar sensor is among the very few throughout the world known to achieve both standards.

Just like 'pixels'

"Hot spots are the key elements in a SERS sensor, as they resolve the spectroscopic fingerprints of the target molecules. They are like pixels in a display that resolve different parts of an image. However, hot spots cannot be seen with the naked eye since their dimensions are only several to tens of nanometers," says Kaiyu Wu.

The aim of Kaiyu Wu's PhD project, which finished recently in June 2016, was to engineer "pixels," i.e., hot spots in the nanopillars in order to take their sensing performance to the next level. This goal was achieved with the help of advanced spectroscopic and theoretical tools, as well as state-of-the-art nanofabrication techniques at DTU Nanotech and DTU Danchip.

The nanopillar sensors can be easily paired with portable read-out systems to enable on-site detection of analytes. Furthermore, their high-quality and high-density hot spots guarantee an extra-high sensitivity which reduces the time of detection to just several seconds for regular targets.

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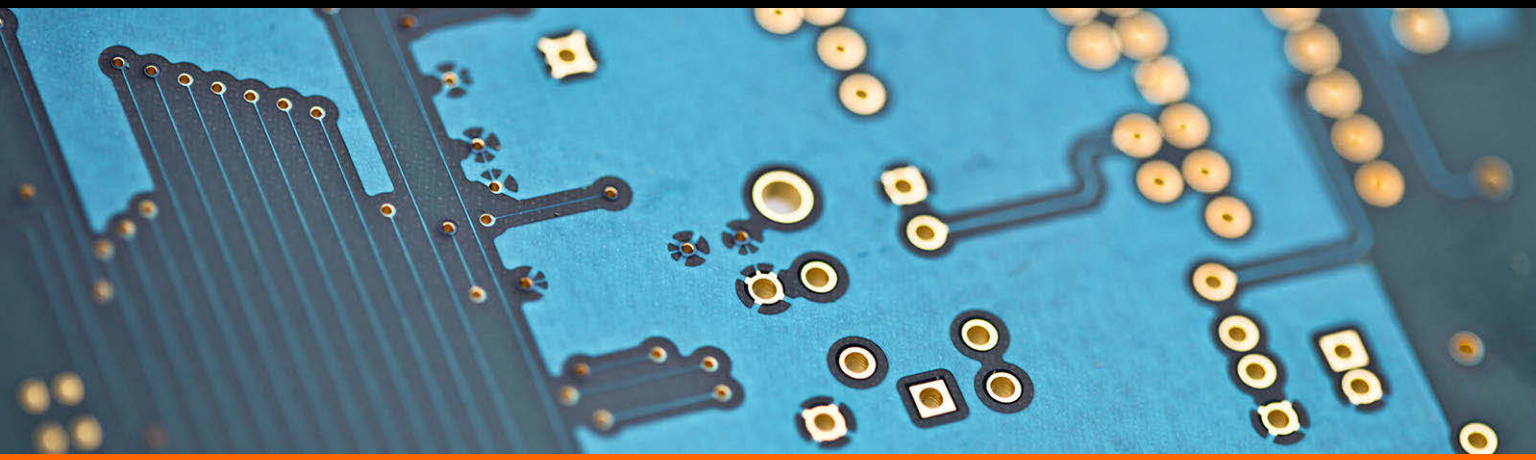

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SUNSTONE CIRCUITS Makes Shift in Strategy, Offerings

by Barry Matties

Sunstone Circuits, the Oregon-based online vendor of quickturn circuit boards, has recently made a shift in capabilities that will enable a move into the RF and microwave space. At PCB West, I caught up with Sunstone's David Warren, and we discussed details of this change and how they plan to approach such a competitive marketplace.

***Barry Matties:** Just to get started, tell us a little bit about Sunstone and specifically, what you do, David.*

David Warren: I'm the sales and business development guy at Sunstone Circuits. I've been with the company for seven years now. I've spent my entire career in manufacturing management and sales within the electronics industry. The majority of my experience revolved around printed circuit board assembly until coming here in 2010. We've been in business for nearly 45 years. We were the first to pioneer online quoting and ordering of PCBs. PCBExpress.com and PCBPro.com were the first websites that allowed for online quoting and ordering. We also have our own proprietary PCB design and layout software, PCB123, allowing both schematic capture and the design and layout of PCBs.

***Matties:** You've had that software out for quite a while, but I understand you now have some new offerings coming out?*

Warren: Yes. This past year, we've gotten into the RF & microwave market. As you know with the Internet of Things, everything's going Bluetooth, RF or microwave. Typically, RF is anything above 100 megahertz, and then microwave would be 2 megahertz and above. It's a totally different animal than your standard FR-4 circuit board.

RF and microwave PCBs have been on our roadmap for quite a while, and earlier this year we jumped into that world with both feet to help some customers out of a bind. This actually has been a great learning experience for us. We have added equipment, updated processes and added technical resources to help us be successful. In less than a year we have come a long way in the RF PCB field and now we feel that

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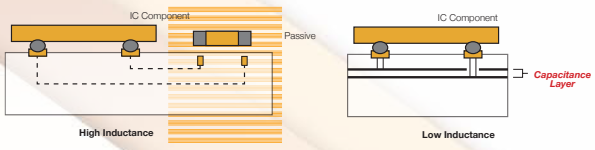

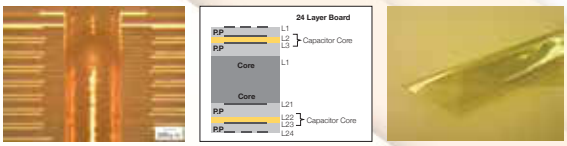

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***Matties:** If you fast-forward to today, what's the result of all of that?*

Warren: Well, we've already exceeded our targets in terms of sales on the RF side of the business for 2016. Like I said, RF and microwave is a different beast—a different material, but Sunstone has the people to make it successful.

***Matties:** When you talk about RF, are you talking about actually manufacturing RF boards? Because that would be new, compared to what you guys have been doing.*

Warren: Correct, we have added customers in the communication, testing and wireless space that require the use of high frequency low loss materials. With these designs, there is a lot tighter dimensional tolerancing for the board and internal routs. Tighter control on line widths, spacing and registration, surface finish requirements, material movement and more.

> "With these designs, there is a lot tighter dimensional tolerancing for the board and internal routs."

***Matties:** All the manufacturing issues come into play, right?*

Warren: Yes. It's a totally different material compared to FR-4. You have the 3000, 4000, 5000, 6000 materials. Some of the materials are almost like working with Silly Putty. The material moves when subject to heat and mechanical processes, and the thickness of the material presented new and challenging handling and conveying processes. Previously the thinnest Rogers material board that we were building was on 20 mil Rogers 4350, which is a fairly rigid material. Now we're down to sub 3-mil Duroid materials with no rigidity.

***Matties:** How does this change the product mix for you? Sunstone was well known for being an online vendor, but this is not necessarily an online purchase. People that are buying RF boards probably need more service or more communication.*

Warren: The reason we got into quickturn online was to differentiate ourselves in a new and disruptive way. We knew we couldn't compete with offshore pricing, especially for volume. We're just not a big facility. On the other hand, we have a great team; the average tenure of our employees is about 13.5 years, and we knew that the offshore people couldn't compete with our extreme customer service, our experience and our ability to rapidly turn quickturn prototypes at a competitive price. They couldn't compete with the short lead times, the service and our ability to do it day after day with world class quality and on time delivery. Now with the addition of the RF product and the complexity of PCBs increasing, we're responding by adding resources to our sales and support teams that will be able to communicate with the engineers and be able to see issues early in the process that could get overlooked in a 'run as sent' online order.

***Matties:** The problem I always see with online customers is you don't have a great relationship with the customer. You have a relationship with their credit card number.*

Warren: This is true, but we're taking a different approach now. We're changing our sales and support structure to be more responsive to customers, adding the personal relationship building with our customers to evolve our partnership to a more productive two way street model. From the customer's perspective, when you're doing business with a company, your livelihood is on the line. You want to make sure they're going to get the job done for you. Our quality rating is consistently within the 99.5% plus range.

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Our on-time delivery is right up there as well. We also have, I think, the only on-time guarantee for quickturn PCBs or your money back with no questions asked, in the industry. We looked at this market we're in and it's a good market for us because we have the reputation of great quality and on-time delivery. They just know what they're going to get.

***Matties:** With RF though, you don't necessarily expect people to be ordering that online.*

Warren: No, not at this time.

***Matties:** This is a real change in business model for you guys.*

Warren: Correct.

***Matties:** Previously, I remember talking to your CEO, Terry Heilman, and he was always touting the fact that you really didn't have a sales force—that sales were all done through marketing, so to speak. This new strategy requires a sales force, more outside account managers, that sort of thing. How's that transition working in the company?*

Warren: It's working pretty well. We're still in the early phases of development, but we're confident that the customers will be very happy.

***Matties:** You're new to the RF game. Why would they go with you over somebody who's been doing it for 10 years?*

Warren: What's really interesting on that is that they may be doing it for 10 years and have a pretty good niche, but we are positioned to be able to service a larger breadth of products for these customers (prototypes to production for FR-4 type of products, as well as the RF circuits). There are not a lot of manufacturers that can be great at both ends of the spectrum and Sunstone is. The experience of our employees, our engineering and our overall support made this transition easy and successful.

***Matties:** Right, I don't question the quality of your crew. I'm just looking at it from the perspective that, if you're in sales, that's a tough hill to climb, because RF is the space everybody's going after. So I'm curious about the strategy or how you overcome that. Everyone's going to say we have great service, we have great quality. That's the cost of entry. If you don't do those things you're not going to be in business, right? You guys have been in business so I understand that you can do that. Can you do it in the RF space?*

Warren: I believe we can. I believe that the customers that we've picked up thus far and have put their faith in us as a supplier have been pretty impressed. We will continue to improve its processes and comfort level with the RF product as new challenges arise. I don't think the competition's really solid out there in the RF space or otherwise they would have gone somewhere else in the first place.

"We will continue to improve its processes and comfort level with the RF product as new challenges arise."

***Matties:** I've talked to other companies out there that have been doing this for a number of years and they're really aggressive; they have boards, and they have a lot of traction in that space. I think it's a smart move on your part. Don't get me wrong. I'm just curious because it's a real shift in your entire strategy.*

Warren: It is, but you have to constantly evolve. You adapt or die. Like when we saw all the high-volume manufacturing going offshore. We adapted and went to quickturn prototypes. We listen to our customers, and listen to what their needs are. Then, we make adjustments to our game plan as we go along to fulfill their needs. The industry is changing. Sunstone has gotten to where they are today for one simple reason: "Do what you do and do it better than

anyone else." Now we're down to online 5 mil space and trace. Ten to 12 years ago some of the capabilities we have would have been unthinkable. This is actually interesting because RF is a lot tighter tolerancing; it's actually enabled us to improve our processes and tighten up our capabilities for tighter tolerances for our previously existing product offering as well.

***Matties:** Across all the panels, which is great.*

Warren: Definitely.

***Matties:** As I'm sitting here thinking about this, RF is new in a lot of areas, right? We're seeing it in automotive and places that you've never really seen it before, and it's starting to trickle down into household appliances even. There's probably a large sector of customers who have never really had to purchase RF boards before. To me, that would be my strategy. Where are the ones that are birthing into this right now? Because then you can grow together.*

David Warren

Warren: We have support staff in place that can take an RF concept drawn on a napkin and help the engineer get what he or she is looking for.

***Matties:** They don't have the history of another manufacturer, they're looking for knowledge, they know that they need to evolve their product, and to me, that might just be the lowest hanging fruit while you're climbing up this hill. It's not the tier 1's. You might be dealing with tier 3, but that hill climb gets you to tier 1.*

Warren: A lot of the business we have is from word of mouth from our initial set of customers to reach out to that existing supplier base and go through the qualification process to get the opportunity to work with them. It's been a steep learning curve, I'll admit that, but I think when you look at it that there's a lot of products out there, industry-wide, that people haven't even thought about the application for RF yet.

***Matties:** Maybe it's just educating them on the concepts of what's available with RF versus specific product design.*

Warren: That's true too, because there are a lot of customers of ours that have never really thought of RF before. It's all new to them.

***Matties:** You're in a great position to be a teacher as much as you are a student.*

Warren: That's why I always tell our sales and customer service teams that they've got to be a resource. You're not always going to get the sale the first time you talk to a customer, but if you prove yourself as a valuable resource, they're going to come back.

***Matties:** It circles back. A "no" is simply not now.*

Warren: I'm a firm believer in that.

***Matties:** So am I. How long have you been in the industry now?*

Warren: 30+ years.

***Matties:** I'm right there. I started in '84.*

Warren: '81 for me.

***Matties:** David, thank you for taking time to speak with me today.*

Warren: My pleasure. **PCBDESIGN**

TOP TEN

Recent Highlights from PCBDesign007

1 Mentor Graphics' PADS Platform Bridges Design and Manufacturing

At PCB West, Publisher Barry Matties spoke with Paul Musto, marketing director for Mentor Graphics' Systems Division, about Mentor's PADS Product Creation Platform and their introduction of scalable software tools to help design better boards, from the enterprise level down to the entry level and hobbyists.

2 Advanced Circuits Upgrades its Free PCB Design Software, PCB Artist 3.2

Advanced Circuits has released version 3.2 of its free professional-grade PCB design software, PCB Artist, the most active PCB software on Downloads.com with over 265,000 downloads. Since its first release in June of 2007, Advanced Circuits' PCB Artist has become well known in the printed circuit board industry as the best free PCB design software.

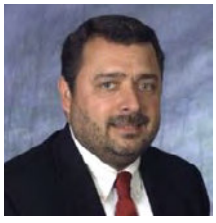
3 SnapEDA: Inspiring Millennials in the PCB Design Community

Natasha Baker, founder of SnapEDA, is part of the new breed of entrepreneurs. She manages a group of millennials who are not much younger than she is, and the company aims to change the way PCB designers use PCB footprints and schematic symbols.

4 Freedom CAD: Navigating the Unpredictable Design Marketplace

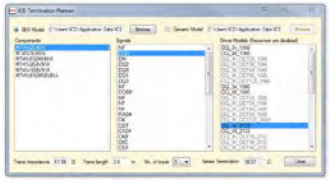
As COO of the design service bureau Freedom CAD, Scott Miller has a front-row seat to the challenges currently plaguing designers and the design community as a whole. He shared his view of the industry with me recently, offering insights on the importance of picking the right partners and customer relationships in an unforgiving and sometimes unpredictable design marketplace.

5 EMA Puts SiliconExpert Part Insight Into OrCAD Design Environment, Reducing Supply Chain Risk



"Our customers can now select parts based on component lifecycle status, environmental compliance, inventory and more all without leaving the OrCAD design environment," said Manny Marcano, president and CEO of EMA. "This capability alone has the potential to save weeks of manual part research, while ensuring that parts with the required specifications are used in the designs."

6 ICD Adds Termination Planner to Stackup Software



In-Circuit Design Pty Ltd (ICD), Australia, developer of the iCD Stackup and PDN Planner software, has released a new Termination Planner feature for its Stackup software. This new feature will be delivered to current ICD support customers as part of an interim upgrade.

7 Beyond Design: How to Handle the Dreaded Danglers, Part 2

In Part 1 of this series, I deliberated on how dangling via stubs distort signals passing through an interconnect and also decrease the usable bandwidth of the signal. This is due to the via stub acting as a transmission line antenna. The conventional solution is to back-drill the vias to bore out the via stub barrels, so that the via stubs are reduced in length if not completely removed. This month I will look into all the possible solutions to alleviate this issue.

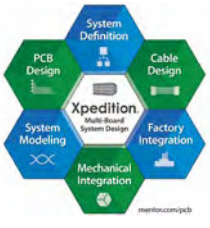
8 Altium ActiveRoute Debuts at PCB West: Routes Under One Second Per Connection

While at PCB West in Santa Clara in mid-September, Judy Warner sat down with Charles Pfeil of Altium to learn more about their exciting new tool, ActiveRoute, that was introduced and demonstrated in their booth during PCB West 2016. She also learned a bit about Pfeil, who is a living history lesson in PCB design.

9 Sunstone Circuits Launches New Version of PCB123 and PCB123.com

Sunstone Circuits has launched a two-part solution for the PCB design engineer: the new version of PCB123, V5.4, and the new PCB123.com. The site has been completely rebuilt to coincide with the new software launch. Now, PCB123 users can use a separate and focused website for PCB123 tool downloads, manuals, tutorials, updates, news, and access to forums.

10 Mentor Graphics Launches Xpedition Multi-Board Systems Design Solution



Mentor Graphics has announced its new Xpedition multi-board systems design solution which enables seamless concurrent multi-discipline team collaboration to efficiently manage increasing system complexity. The Xpedition flow maximizes team efficiency by eliminating redundant effort during the design process.

PCBDesign007.com for the latest circuit design news and information—anywhere, anytime.

Events

For IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out The PCB Design Magazine's event calendar.

Electronica
November 8–11, 2016
Munich, Germany

FUTURECAR: New Era of Automotive Electronics Workshop
November 9–10, 2016
Atlanta, Georgia, USA

Printed Electronics USA
November 16–17, 2016
Santa Clara, California, USA

IMPACT Europe 2016
November 29, 2016
Brussels, Belgium

ICT-UK Evening Seminar
December 1, 2016
Harrogate, North Yorkshire, UK

International Printed Circuit & Apex South China Fair (HKPCA)
December 7–9, 2016
Shenzhen, China

DesignCon 2017
January 31–February 2, 2016
Santa Clara, California, USA

MD&M West
February 7–9
Anaheim, California, USA

IPC APEX EXPO 2017 Conference and Exhibition
February 14–15, 2017
San Diego, California, USA

China International PCB & Assembly Show (CPCA)
March 2017
Shanghai, China

Thailand PCB Expo 2017
May 11–13, 2017
Bangkok, Thailand

JPCA Show 2017
June 7–9, 2017
Tokyo, Japan

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